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Hybrid HVDC Transformer for Multi-Terminal Networks

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IDCORE

This Thesis is submitted in partial fulfilment of the requirements for the award of an Engineering Doctorate, jointly awarded by the University Edinburgh, University of Exeter and the University of Strathclyde. The work presented has been conducted under the supervision of The Offshore Renewable Energy Catapult (ORE Catapult) as a project within the Industrial Doctoral Centre for Offshore Renewable Energy.

Declaration

I declare that this thesis was composed by myself and that the material presented, except where clearly indicated, is my own work. I declare that that the work has not been submitted for consideration as part of any other degree or professional qualification. Any included publications are my own work.

Abstract

There is a trend for offshore wind farms to move further from the point of common coupling to access higher and more consistent wind speeds to reduce the levelised cost of energy. To accommodate these rising transmission distances, High Voltage Direct Current (HVDC) transmission has become increasingly popular. However, existing HVDC wind farm topologies and converter systems are ill suited to the demands of offshore operation. The HVDC and AC substations have been shown to contribute to more than 20% of the capital cost of the wind farm and provide a single point of failure. Therefore, many wind farms have experienced significant delays in construction and commissioning, or been brought off line until faults could be repaired. What is more, around 75% of the cost of the HVDC and AC substations can be attributed to structural and installation costs. Learning from earlier experiences, industry is now beginning to investigate the potential of a modular approach. In place of a single large converter, several converters are connected in series, reducing substation individual size and complexity. While such options somewhat reduce the capital costs, further reductions are possible through elimination of the offshore substations altogether.

This thesis concerns the design and evaluation the Hybrid HVDC Transformer, a high power, high voltage, DC transformer. This forms part of the platform-less (i.e. without substations) offshore DC power collection and distribution concept first introduced by the Offshore Renewable Energy Catapult. By operating in the medium frequency range the proposed Hybrid HVDC Transformer can be located within each turbine's nacelle or tower and remove the need for expensive offshore AC and DC substations.

While solid state, non-isolating DC-DC transformers have been proposed in the literature, they are incapable of achieving the step up ratios required for the Hybrid HVDC transformer [1]–[3]. A magnetic transformer is therefore required, although medium frequency and non-sinusoidal operation does complicate the design somewhat. For example, inter-winding

capacitances are more significant and core losses are increased due to the added harmonics injected by the primary and secondary converters [1], [2].

To mitigate the impact of these complications, an investigation into the optimal design was conducted, including all power converter topologies, core shapes and winding configurations. The modular multilevel converter in this case proved to be the most efficient and practical topology however, the number of voltage levels that could be generated on the primary converter was limited by the DC bus voltage. To avoid the use of pulse width modulation and hence large switching losses, a novel MMC control algorithm is proposed to reduce the magnitude of the converter generated harmonics while maintaining a high efficiency.

The development and analysis of this High Definition Modular Multilevel Control algorithm forms the bulk of this thesis' contribution. While the High Definition Modular Multilevel Control algorithm was developed initially for the Hybrid HVDC Transformer, analysis shows it has several other potential applications particularly in medium and low voltage ranges.

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List of Publications

Presentations

M. Smailes, C. Ng, P. McKeever, "High Definition MMC for platform-less HVDC offshore wind power collection system", presented at Wind Europe, Hamburg, 2016

M. Smailes, C. Ng, R. Torres-Olguin, P.Paradell, J. L. Dominguez-Garcia, G. Guidi, K. Ljøkelsøy, S. D'Arco, "Experimental Validation of High Definition Modular Multilevel Converter", IRPWind workshop on novel technologies for offshore wind power integration, Barcelona, 2017

M. Smailes, C. Ng, R. Torres-Olguin, P.Paradell, J. L. Dominguez-Garcia, G. Guidi, K. Ljøkelsøy, S. D'Arco, "Experimental Validation of a High Definition Modular Multilevel Converter for HVDC Converters", Offshore European Wind, London, 2017

Conference Publications

M. Smailes, C. Ng, J. Shek, M. Abusara, G. Theotokatos, and P. McKeever, "Hybrid, multi-megawatt HVDC transformer for future offshore wind farms," in *Renewable Power Generation Conference (RPG 2014), 3rd*, 2014, pp. 1–6.

M. Smailes *et al.*, "Evaluation of core loss calculation methods for highly nonsinusoidal inputs," in *11th IET International Conference on AC and DC Power Transmission*, 2015, pp. 1–7.

M. Smailes, C. Ng, P. McKeever, R. Fox, M. Knos, and J. Shek, "A modular, multi-megawatt, hybrid HVDC transformer for offshore wind power collection and distribution," in *EWEA Offshore Wind Energy Conference 2015*, 2015.

Journal Publications

M. Smailes, C. Ng, P. Mckeever, J. Shek, G. Theotokatos, and M. Abusara, "Hybrid, Multi-Megawatt HVDC Transformer Topology Comparison for Future Offshore Wind Farms," *Energies*, vol. 10, no. 7, p. 851, Jun. 2017.

Patents

C. H. Ng, P. Mckeever, and M. E. Smailes, "Power Converter," WO/2016/181155, 18-Nov-2016.

Successful European Funding Applications

Experimental Validation of High Definition Modular Multilevel Converter in IRPWind project – first Call for Joint Experiments Work programme 2016 April 2016.

Grid Integration of High Definition Modular Multilevel Converter, second Call for Joint Experiments Work programme 2016, February 2017.

National Funding Reports

Next Generation HVDC Network for the Offshore Renewable Energy Industry – prepared for TSB (InnovateUK), December 2014

European Funding Reports

High Power Definition Modular Multilevel Converter – prepared for IRPWind project – first Call for Joint Experiments, Work programme 2016, February 2017

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Abbreviations

[a b c]	Number of sub-modules in set a, set b and set c
{a b c}	Number of sub-modules to be switched on in set a, set b and set c in the next time step
AC	Alternating Current
APOD	Alternative Phase Opposite Disposition
A/D	Analogue to Digital converter
B2B	Back to Back
C-MMC	Conventional Modular Multilevel Converter
C-PWM	Carrier Pulse Width Modulation
CB	Circuit Breaker
CCS	Circulating Current Suppressor
C_{dc}	Direct Current Capacitor
CHB	Cascade H-Bridge
C_n	Lower Arm Capacitor
C_p	Upper Arm Capacitor
CUT	Core Under Test
DC	Direct Current
DC/DC	Back to Back Direct Current Converter
D_n	Lower Arm Diode
D_p	Upper Arm Diode
dq0	Direct quadrature-zero
DRU	Diode Rectifier Unit
EMF	Electromotive Force
EMI	Electromagnetic Interference
FB	Full Bridge
FB-FB	Full Bridge converter on primary and secondary side of the transformer
FB-MMC	Full Bridge converter on primary and Modular Multilevel Converter on the secondary side of the transformer
FCC	Flying Capacitor Converter
FFT	Fast Fourier Transformer
FPGA	Field Programmable Gate Array
FT	Fourier Transform
FTSE	Fourier Transform Steinmetz Equation
GSE	General Steinmetz Equation
HD-MMC	High Definition Modular Multilevel Converter
HF	High Frequency
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current

IDCORE	Industrial Doctoral Centre for Offshore Renewable Energy
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commuted Thyristor
iGSE	Improved General Steinmetz Equation
IREC	Institut de Recerca en Energia de Catalunya
L	Level
LCC	Line Commutated Converter
LV	Low Voltage
M	Million
MF	Medium Frequency
MFPT	Medium Frequency Power Transformer
MMC	Modular Multilevel Converter
MMC-FB	Modular Multilevel Converter on the primary and Full Bridge on the secondary side of the transformer
MMC-MMC	Modular Multilevel Converter on the primary and secondary side of the transformer
MOSFET	Power Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
MSE	Modified Steinmetz Equation
MV	Medium Voltage
MVDC	Medium Voltage Direct Current
NAREC	National Renewable Energy Centre
NLM	Nearest Level Modulation
NPC	Neutral Point Clamp
O&M	Operation and Maintenance
ORE Catapult	Offshore Renewable Energy Catapult
PA	Power Analyser
PCC	Point of Common Coupling
PD	Phase Disposition
POD	Phase Opposite Disposition
PSC	Phase Shift Carrier
PWM	Pulse Width Modulation
RL	Resistive Inductive load
RMS	Route Mean Square
S_b	Bypass Switch
SE	Steinmetz Equation
SINTEF	Stiftelsen for Industriell og Teknisk Forskning
SM	Sub-Module
STATCOM	Static Synchronous Compensators
SVM	Space Vector Modulation
S_w	Switch
V	Valve
V_n	Lower Arm Valve
V_p	Upper Arm Valve
VSC	Voltage Source Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Nomenclature

Roman Upper Case

A	Carrier wave amplitude
A_e	Core cross sectional area
A_c	Core area
$A_{winding}$	Winding area
B	Flux density
$\hat{B}$	Peak flux density
B_R	Residual magnetism
B_{pk}	Peak flus density
B_{sat}	Saturation flux density
C_{arm}	Arm capacitance
C_f	Filter capacitance
$\check{C}_{mod}$	Minimum allowable sub-module capacitance
D	Duty ratio
D_c	Depth of the core
D_t	Turbine Diameter
E_{arm_0}	Initial arm energy
E_{arm}	Arm energy
EP	Energy Power Ratio
H	Magnetic field strength
H_c	Coercive Force
H_c	Height of the core
H_w	Window core height
I_c	IGBT rated collector current
$\hat{I}_j$	Peak nominal AC terminal current
J	Winding current density
$\hat{J}$	Maximum current density
K_p, K_i	Proportional and integral PI constants
L_0	MMC arm inductance
L_T	Transformer inductance
L_c	Length of the core
L_e	Effective core length
L_f	Filter capacitance
L_{grid}	AC grid inductance
L_l	Load reactance
L_w	Window core length
$\check{L}_0$	Minimum allowable arm inductance

M	Modulation index
N_D	Number of clamping diodes per branch
N_c	Number of carrier waves
N_{cap}	Number of flying capacitors
N_{cap}	Number of sub-module capacitors per arm
N_p, N_s	Primary and secondary number of turns
N_{sw}	Number of switches
N_w	Number of winding turns
N_w	Number of winding turns
P	Active power
P_{hyst}	Hysteresis power loss
P_T	Power transferred across a reactance
P_{arm}	Stored power in an arm of the MMC
P_{con}	Converter conduction losses
P_{core}	Magnetic core power loss
P_{ed}	Eddy current power loss
P_p	Primary winding loss
P_{rr}	Reverse recovery loss
P_s	Secondary winding loss
P_{sw}	Switching loss
P_{sw}	Converter switching losses
P_{tot}	Total converter loss
Q	Reactive power
R_0	Equivalent arm resistance
R_{FE}	Equivalent magnetic losses resistance
R_{ac}	Winding AC resistance
R_{dc}	DC winding resistance
R_f	Filter Resistance
R_l	Load resistance
R_{on}	IGBT on resistance
R_p	Primary winding resistance
R_s	Secondary winding resistance
R'	Combined resistances referred to primary
SM_{dr}	SM driver signal
SM_{max}	Maximum change in the number of SMs inserted
SM_{mean}	Average maximum change in the number of SMs inserted for all voltage levels
SM_{nom_y}	Normalised, SM_{mean} for the number of SMs in the yth Set
SM_{omit}	Number of sub-modules omitted in a cycle
S_{com}	Possible set combinations
S_f	Safety factor
T_{cycle}	Cycle period
T_{gap}	Thickness of the gap between each phase
THD	Total Harmonic Distortion
T_{in}	Thickness of the insulation layer between the bobbin and primary winding
T_o	Period of the oth cycle
T_{out}	Thickness of the insulation layer surrounding outside of the secondary winding

T_p	Thickness of the primary copper foil
T_{pi}	Thickness of the primary winding insulation
T_{ps}	Thickness of the insulation layer between the primary and secondary windings
T_{si}	Thickness of the secondary winding insulation
U_L	Voltage between each secondary layer
U_{Sy}	Nominal voltage for the yth Set
U_c	Nominal SM capacitor voltage
U_{ces}	IGBT rated collector emitter voltage
U_{dc}	DC Voltage
U_{dc_p}	Primary DC voltage
U_{dc_s}	Secondary DC voltage
U_{mod}	Cascade H-bridge's module voltage
U_{ps}	Voltage between last turn of primary winding and first of secondary winding
U_{ry}	Ratio of the SM from the yth Set to the first Set
U_s	Nominal set voltage
$\widehat{U}_j$	Peak nominal AC terminal voltage
V_T	Volume of the transformer
V_c	Core volume
V_{ce}	Collector emitter voltage
V_{core}	Volume of the core
W_d	Width of the smallest perpendicular dimension of the core to the flux path
X'	Combined reactances referred to primary
X_M	Magnetising reactance

Roman Lower Case

a	Turns ratio
d_c	Diameter of the secondary copper core
d_w	Winding diameter
d_w	Diameter of secondary winding including insulation
e_d, e_q	dq0 transformation of the inner EMF
e_j	Inner EMF
f_0	Reference operating frequency [Hz]
f_{cr}	Carrier wave frequency
f_s	Sampling frequency
g	Number of Sets
h_{max}	Maximum harmonic number
h_p	Height of the primary foil winding
i_0	Magnetic loss current
i_{arm}	Arm current
i_{arm}	Arm current
i_c	Collector current
i_d, i_q	dq0 transformation of the phase current
i_{dc}	DC converter current
i_{dc_p}	Primary DC bus current

i_{dc_s}	Secondary DC bus current
i_{fj}	Filter current for the j^{th} phase
i_j	Phase current
i_l	Cycle number
i_{nj}	Lower arm current
i_o	Set configuration option number
i_p, i_s	Primary and secondary current
i_{pj}	Upper arm current
i_{pj_i}	Individual SM current
i_s	Switch number
i_t	Time step number
i_w	Winding current
$i_{\Delta d}, i_{\Delta q}$	dq0 transformation of the difference current
$i_{\Delta j}$	Difference current
j	Phase (a, b, c)
k_{SE}, α, β	Steinmetz parameters
k_{iGSE}	iGSE constant
k_s	Core shape constant
k_w	Weighting factor
l	Magnetic path length
l_w	Mean length of winding
m	Number of sub-modules per arm
mmf	Magneto motive force
n	Number of voltage levels
n_c	Number of waveform cycles
n_l	Number of layers in the secondary
n_{pj_i}	Individual SM insertion index
n_{rd}	Number of redundant states per cycle
n_{st}	Number of time steps
n_{st}	Number of Set states per cycle
n_t	Number of turns per layer in secondary
n_v	Number of valves
o	Loop number
p_o	Magnetic core loss for major or minor sub loop
q_f	Quality factor of filter
r_{bob}	Radius of the bobbin
r_{in}	Distance from centre of bobbin to primary winding
r_p	Primary winding radius
r_s	Outer radius of the secondary winding
r_w	Radius of secondary winding including insulation
s	Number of switches per arm
t	Time
$u_{c_{0,}i_m}$	Carrier wave DC offset
u^*	Modulation reference waveform
u_D	Diode voltage stress
u_c	MMC's sub-module voltage
u_c'	Revised SM voltage including weighting factor
u_{ccs}	Output of the CCSC
u_{ce}	Collector emitter voltage

u_{cpj_i}	Individual SM voltages
u_f	Forward voltage
u_j	Phase voltage
u_{lz}	Induced EMF due to Lenz's Law
u_{mod}	Modulated voltage waveform
u_{nj}	MMC's lower arm voltage
u_p^*, u_n^*	Reference modulator waveforms for upper and lower arms
u_p, u_s	Primary and secondary voltage
u_{pj}	MMC's upper arm voltage
u_{ref}	Magnitude of the reference waveform
u_s'	Referred secondary voltage
u_{sy}	Voltage of the yth Set
u_w	Winding voltage
v	Valve number
y	Set number
y_h	Harmonic magnitude

Greek

η_m	Number of SMs inserted in current path
η_m	SM's current state 1 = in, 0 = out
η_{max}	Maximum SMs inserted per cycle
μ_0	Permeability of a vacuum
μ_r	Relative Permeability
ρ_c	Magnetic core's electrical resistivity
ρ_w	Winding resistivity
ς_{ONy}	Number of SMs switched in from the yth Set
ς_y	Number of SMs in the yth Set
ω_0	Reference operating frequency [rad/s]
ϵ_{opi_o}	Error in the i$_o^{th}$ Set configuration option
ϵ_r	Dielectric field strength
ϕ_m	Carrier wave phase
$*$	Control reference value
h	Harmonic number
$\Delta\widehat{U}_j$	Maximum voltage fluctuation for the j^{th} phase
ΔU_{Sy}	Normalised relative voltage deviation of the yth Set
Δu_j	Allowable voltage fluctuation for the j^{th} phase
$\Delta\widehat{E}_{arm}$	Maximum arm energy deviation from initial value
$\Delta\check{E}_{arm}$	Minimum arm energy deviation from initial value
ΔB	Peak to peak flux density
Δu	Percentage voltage deviation from Nominal SM voltage
δ	Skin depth
δ	Angle between the primary and secondary voltage
δB_{i_t}	Change in B over time i_t
δt_{i_t}	Change in time over time i_t
θ	Flux
$\hat{\theta}$	Peak flux
ϑ	Phase angle

Chapter 1 Introduction

1.1 Overview and Introduction to the Research Topic

Offshore wind is under continued pressure to reduce its levelised cost of energy and become cost competitive with other forms of energy generation. To this end, wind farms have both moved further offshore to access greater and more consistent wind velocities and increased in size to realise cost reduction through economies of scale [4]–[10] as illustrated in Fig. 1.1.

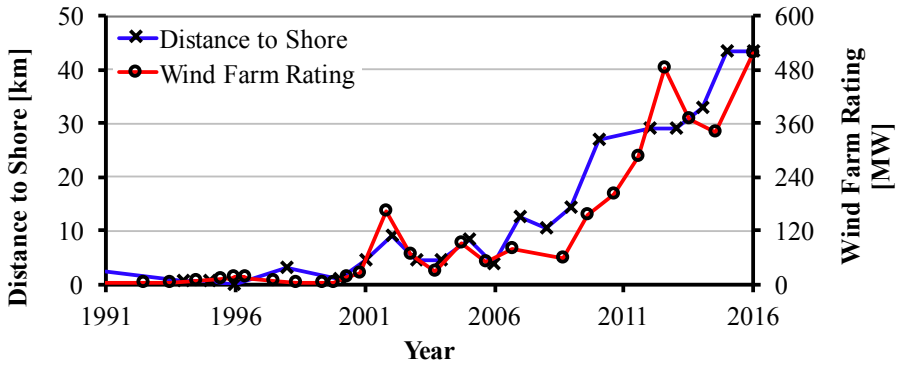


Fig. 1.1 Average distance to shore and rated capacity of connected wind farms for each year [4]–[10]

Globally, the majority of offshore wind farms have been connected to the Point of Common Coupling (PCC) through High Voltage Alternating Current (HVAC) transmission cables. These cables are known to have very high parasitic capacitances proportional to their distance, requiring extensive reactive power compensation. Over long distances, the reactive compensation must be staggered over the cable length as shown in Fig. 1.2, requiring the construction of additional offshore platforms. Furthermore, the voltage of long cables is restricted and large wind farms far from the PCC require several parallel HVAC transmission

cables. As a result, HVAC cable transmission becomes economically untenable over long distances and High Voltage Direct Current (HVDC) becomes preferred as depicted in Fig. 1.3.

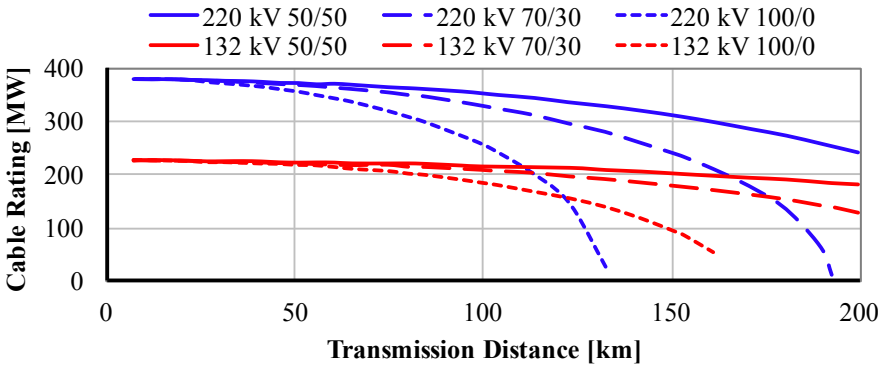


Fig. 1.2 Rated power of AC submarine cables vs. distance with different reactive power compensation scenarios [11]

High Voltage Direct Current (HVDC) transmission does not suffer from inductive or capacitive effects and as such, does not require reactive compensation. Additionally, more than the same amount of power can be transferred through two cables in place of three AC cables for a given voltage and current rating further reducing the per unit distance cost of HVDC transmission [12]. However, large and expensive HVDC substations are required at either end of the transmission cable though. There is therefore a critical distance, above which, HVDC becomes more economical than HVAC as shown in Fig. 1.3.

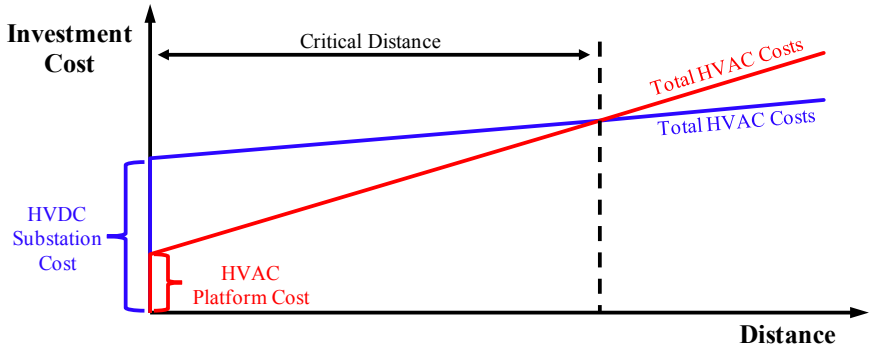


Fig. 1.3 The economic cross over point between HVAC and HVAC transmission. [13]

The first generation of offshore HVDC substations were based on onshore HVDC converter designs. Each had a mass in the region of 10,000 to 20,000 tonnes and contributed to around 15 – 25% of its capital cost [14]–[16]. Of this total, the converter only accounts for around 25%, with the remaining costs attributed to structural, installation and ancillary costs. This leaves great scope to potentially reduce the wind farm's cost and simplify its construction and installation [17]. Furthermore, the substation also presents a single point of failure or project

delay, which has already caused TenneT serious technical and financial problems [18], [19]. Clearly then, the existing topology is not optimised for the offshore environment and an alternative approach should be sought.

To this end, The Offshore Renewable Energy Catapult (ORE Catapult) (previously the National Renewable Energy Centre (NAREC)) introduced the Hybrid HVDC Transformer concept in 2009 [20]. It was proposed that the Hybrid HVDC Transformer could be located within the wind turbine's nacelle or tower, directly stepping up the voltage to HVDC for transmission. In this way, the offshore substations could be eliminated, thus reducing the cost of offshore wind farms. In so doing, the system redundancy would also be improved, since if a converter module were to fail, only one turbine would be affected.

The work in this thesis further develops the Hybrid HVDC Transformer concept and builds on the initial feasibility study presented in [20]. It focuses on identifying and solving the technical challenges to implementing the concept culminating in a proposed topology and novel converter control strategy.

1.2 Previous Works

The potential cost reductions offered through a more modular approach to HVDC conversion in offshore wind farms has sparked increasing interest in both academia and industry. The most recent offshore wind farm design proposed by Siemens, the Diode Rectifier Unit (DRU), replaces the offshore AC and DC substations by several, smaller DRU platforms [21]. While some cost reductions can be expected through this strategy, further improvements could be made by eliminating the offshore platforms completely.

To this end, several non-isolating DC transformer concepts have been proposed in [1], [2], [22]–[24]. In place of magnetic transformers, the voltages are stepped up through resonant interactions between the converter's capacitor and inductor banks. Such designs are generally smaller and lighter than traditional 50 Hz transformers and avoid the complications involved in designing Medium (61 to 2000 Hz) or High (>2000 Hz) Frequency (MF or HF) transformers [1]–[3]. However, the achievable step up ratios are too low to reach the voltages required for HVDC transmission.

The step up ratios of magnetic transformers are not as restrictive, and several MF designs for the offshore wind industry have been proposed [25]–[30]. These designs still utilise relatively low turns ratios connecting instead to Medium Voltage DC (MVDC) grids or relying on large numbers of series connected turbines to reach HVDC levels. In doing so, the converter design

is simplified as the voltage and current remain within the normal operating range of standard semiconductor switch ratings. Moreover, since both converters experience relatively low voltage stresses, traditional, two level (2L) converter topologies such as the Full Bridge (FB) can be used on both the primary and secondary.

Recent developments in multilevel converter topologies, such as the Modular Multilevel Converter (MMC) can provide increases in converter and core efficiencies [31], [32]. These improvements are most notable in HVDC applications where the number of voltage levels are not restricted. To improve the MMC's performance in Low Voltage (LV) and MV applications, methods to increase the number of voltage levels generated have been proposed for various modulation strategies [33], [34]. However, these methods create additional, uncontrollable circulating currents, potentially destabilising the converter operation and reducing its efficiency. An alternative approach proposed in [35] does not generate additional circulating currents however, it is only suitable for low power factor applications such as Static Synchronous Compensators (STATCOMs).

Reducing the magnetic transformer volume by operating in the MF range, increases the power density and hence also loss density. It is therefore important to accurately calculate the magnetic losses. Conventionally, the Steinmetz Equation (SE) is used to calculate core losses; however, this is only valid for sinusoidal flux waveforms [36]. As the DC converters inject additional harmonics, the SE is no longer valid. A common approach in industry is to take the Fourier Transform (FT) of the flux and use the SE with each sinusoidal component (FTSE). This is known to be inaccurate however, due to the non-linearity of the SE. Several alternate approaches have therefore been proposed in the literature, including the use of hysteresis models [37], [38], separation of loss components [39]–[43] and empirical formula [36], [44]–[46]. Of these, the latter is the easiest to calculate since the prerequisite information is generally provided by the core manufacturers [41]. That said, the approach used by industry is still simpler to implement and little work has been done to investigate the reduction in accuracy achieved compared to other empirical calculation methods.

1.3 Research Question, and Scope

Given the need to reduce the cost of offshore wind and the trend for wind farms to move further offshore, a modular HVDC converter system is required. This thesis focuses on solving the technical challenges involved in designing a high power, MF, DC/DC transformer with a high step-up ratio, compact enough to fit within a turbine nacelle or tower.

To this end, the main research objectives are:

- Assessment of core loss equations for non-sinusoidal waveforms based on usability and accuracy
- Comparison of converter topologies to determine suitable configuration for the Hybrid HVDC Transformer
- Development of an analytical loss model to compare different Hybrid HVDC Transformer Configurations and determine key requirements
- An economic assessment and comparison of the Hybrid HVDC Transformer to conventional HVDC collection systems and new approaches proposed by industry.
- Development of a novel High Definition MMC (HD-MMC) control algorithm to improve the performance of the MMC in LV and MV applications.
- Experimental validation and assessment of the HD-MMC.
- Optimisation and operational range of the novel control strategy.

To achieve each of these objectives, a variety of research methodologies have been employed, including computer simulations, mathematical model and control algorithm development, experimental validations and economic analyses as depicted in Fig. 1.4.

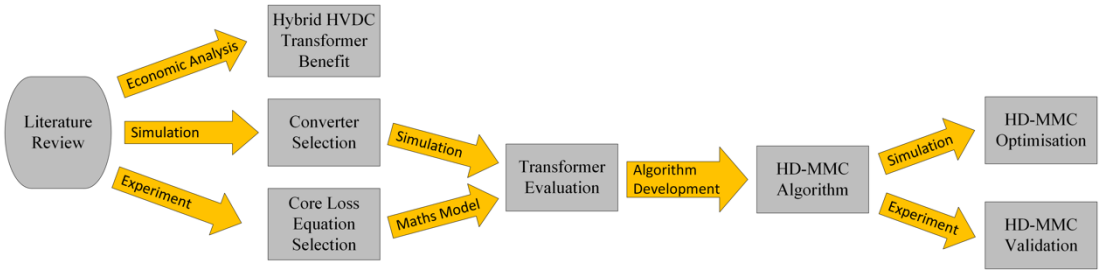


Fig. 1.4 Research methodologies used to reach project objectives

Using conventional and the potential future wind farm topologies proposed in the literature, three, theoretical wind farm models were developed along with a fourth model for the Hybrid HVDC Transformer. The capital costs of each model were calculated using prices gathered from a literature review. The total capital cost of each option was then compared to determine the cost reduction offered by Hybrid HVDC Transformer compared to conventional and potential future wind farm topologies.

Using a literature review, two converter configurations were selected for further study. The FB converter is the most commonly used topology in the literature for MF DC transformers. It is a very mature and robust topology that is well suited to the high current conditions present in the primary converter. The MMC by contrast is a relatively new topology, primarily used in high voltage applications and hence well suited for the secondary converter topology. A detailed MATLAB/Simulink model was therefore developed to evaluate the performance of these topologies for use in the Hybrid HVDC Transformer concept.

The literature review also revealed several methodologies to calculate the core loss of non-sinusoidally excited transformers. The review revealed that, outside of specific simulation packages, empirical methods presented the best trade-off between accuracy and simplicity. Many in industry continue to use the FTSE despite this generally being reported to be less accurate. An experimental analysis was therefore used to determine the relative accuracies between the SE, FTSE and Improved General Steinmetz Equation (iGSE). Using a C-Core Ferrite transformer core, the core losses were calculated under various excitation waveform shapes and compared to the losses predicted by each empirical method.

The results of these experiments and computer models, were then incorporated into an analytical model of the whole Hybrid HVDC Transformer to determine the optimal operating range and configuration of the transformer core.

This analysis revealed that the converter switching losses accounted for a significant proportion of the Hybrid HVDC Transformer losses. To reduce these losses a novel converter control algorithm, the HD-MMC, was developed. This algorithm increases the number of voltage levels created by the MMC for a given converter design. In MV and LV applications, the generated Total Harmonic Distortion (*THD*) of the converter can therefore be reduced without the use of Pulse Width Modulation (PWM), resulting in efficiency improvements.

This was validated through physical experiments performed using SINTEF's research facilities in Norway and independently assessed by IREC in Spain to ensure a fair test. A single-phase, 18 Sub-Module (SM) MMC was operated with an open loop control using different HD-MMC configurations. This was compared to a conventional MMC (C-MMC) using both Nearest Level Modulation (NLM) and Pulse Width Modulation (PWM). The number of switching operations, *THD* and efficiency of each configuration was calculated and used to evaluate the HD-MMC's performance.

A detailed analysis of the HD-MMC was then performed through MATLAB/Simulink simulations. This analysis was used to determine the optimum configuration and operating conditions of the HD-MMC to minimise *THD* and maximise efficiency. The operational range of the HD-MMC and potential improvements to the algorithm were also proposed through use of this model.

1.4 Original Contribution

Based on the objectives and research methodologies outlined in Section 1.3, the original contributions offered by this work can be summarised as:

- An experimental comparison of the SE, FTSE and iGSE to compare the relative accuracies of each method using different frequencies and wave shapes.
- Comparison of different configurations of the FB and MMC configurations in a MF, DC/DC transformer with a very high step-up ratio. This includes a hybrid combination of a FB converter on the primary and MMC on the secondary
- A detailed analytical comparison of different configurations of a MF, DC, high step-up ratio transformer, considering both the converter topology and impact on the magnetic transformer design.
- Development of a novel HD-MMC control algorithm capable of increasing the number of voltage levels generated by a given MMC design. Crucially, this algorithm does not generate any additional circulating currents and is applicable to a wide range of power applications.
- An experimental validation of the HD-MMC algorithm demonstrating its potential advantages over the use of PWM in LV and MV applications
- A detailed analysis revealing the operational range of the HD-MMC, in terms of the carrier wave frequency, modulation index, power factor and circuit configuration.
- Optimisation of the HD-MMC's parameters to maximise efficiency and minimise the *THD*
- Potential methods to extend the operational range of the HD-MMC algorithm
- An economic analysis on the capital cost of the Hybrid HVDC Transformer compared to that of a conventional wind farm topology and two potential future wind farm configurations.
- An independent economic analysis of the DRU concept and a potential future iteration are presented

Many empirical equations to calculate power loss in non-sinusoidally excited cores have been presented in the literature; however, industry continue to use the FTSE. While it has been suggested in the literature that this is less efficient than other options, it is relatively simple to implement. Furthermore, the SE has been validated repeatedly for all core materials and frequencies while the iGSE is comparatively immature. The accuracies of the iGSE and FTSE are therefore compared to the SE to determine the best calculation method for the analysis of the Hybrid HVDC Transformer and determine any penalty in terms of accuracy for using the FTSE.

Numerous DC transformer topologies were found in the review of previous works in this area. However, these focused on relatively low voltage and step-up applications. To maximise efficiency and reduce the capital cost of HVDC connected wind farms, it is necessary to eliminate the offshore HVDC substation. This requires each turbine to export to HVDC and necessitates a high step-up ratio. The large voltage difference between the primary and secondary sides creates unique challenges in the transformer design not considered in other works. Different converter configurations must be considered to withstand the high primary current stresses and secondary voltage stresses while minimising losses and maximising component rating. Therefore, part of this work's contribution is a detailed evaluation of three

transformer configurations. The efficiency and volume of each configuration is calculated over the MF spectrum and a range of winding configurations.

This analysis revealed that the Hybrid HVDC Transformer losses are highly sensitive to switching losses. To reduce the required switching frequency, the HD-MMC was developed to increase the number of voltage levels generated by a MMC in MV and LV applications. This provides a more efficient method to reduce the *THD* compared to using PWM and its experimental validation, optimisation and operational range determination form a significant contribution of this thesis. Crucially, unlike other methods discussed in Section 1.2, the HD-MMC algorithm doesn't create additional circulating currents [33], [34] and is applicable to a wide range of power applications. Such examples include, but are not limited to, Static Synchronous Compensators (STATCOMs), solar farms, aerospace and electric vehicles. As a result, the HD-MMC has attracted much interest, winning 2 European funding calls to undergo experimental validation and is covered by a patent application.

Finally, an economic analysis is performed on the Hybrid HVDC Transformer concept, comparing its capital cost to that of three other wind farm topologies. These include a conventional HVDC wind farm topology, a new topology proposed by industry and a potential future concept.

1.5 Thesis Outline

This thesis is comprised of 7 chapters, a summary of which is outlined below:

Chapter 2: contains the literature review and introduces the key concepts that are developed in this research work. The converter topologies, control strategies, magnetic transformer principles, core loss mechanisms and wind farm topologies strategies are all discussed later in the thesis.

Chapter 3: concerns the detailed evaluation of the Hybrid HVDC Transformer. An assessment of the core loss calculation formulae available in the literature is conducted by comparing the loss predicted by the formulae to that measured in the transformer core itself. The magnetic transformer design and calculation of winding and core losses is then discussed before an analysis of three converter topologies was conducted in the MATLAB/Simulink environment. The results of the converter simulations and magnetic transformer design were combined to determine the overall performance of the transformer for each converter topology over the MF range.

Chapter 4: introduces the operation and implementation of the proposed HD-MMC algorithm. Results presented for an experimental validation of the algorithm not only validate the HD-MMC's operation, but also demonstrate improved efficiency compared to the use of PWM.

Chapter 5: concerns the optimisation of the HD-MMC algorithm and definition of its operational range through use of computer models. A possible method to mitigate these limitations is also presented and discussed.

Chapter 6: contains an economic analysis of an offshore wind farm using a Hybrid HVDC Transformer. This is compared to the capital costs associated with a conventional HVDC offshore wind farm and a new and potential farm topology.

Chapter 7: concludes the thesis, bringing all the concepts together.

Chapter 2 **Literature Review**

The aim of this work is to solve the technical challenges surrounding the design of the Hybrid HVDC Transformer. To that end, it first must be placed in the context of existing works so that the remaining technical challenges and knowledge gaps can be identified. The main aim of this chapter is to present this work and background information in order to guide the rest of the thesis. An additional aim of this chapter is to create a clear distinction between the original contributions of this work and the previous works in the field. As a result, all the background theory for the concepts introduced in the thesis are presented in this chapter. The following chapters will refer to the relevant sections as required.

Given this, the objectives of this chapter are to present the:

- most common converter topologies
- multilevel converter control and modulation strategies
- mathematical model of the MMC
- design requirements for the MMC
- computer modelling techniques for the MMC
- magnetic transformer core and winding design options
- magnetic transformer core and winding loss mechanisms
- conventional wind farm topologies and transmission strategies
- potential future wind farm topologies and conversion strategies

To accomplish these objectives the chapter is organised as follows; common two level (2L) and multilevel converter topologies with an in-depth review of the MMC are presented in Section 2.1. This covers its configuration, control theory and present limitations to reflect the focus of this thesis. Magnetic transformer design is then discussed in Section 2.2, including core shapes, winding configurations, material selection and loss mechanisms. The

conventional and potential future wind farm grid configurations are covered in Section 2.3 and key conclusions are drawn in Section 2.4.

2.1 Converter Topologies

This section covers the most common 2L and multilevel Voltage Source Converter (VSC) topologies used in industry. Their various merits are compared and suitable modulation strategies are discussed. As much of this work centres around the MMC, it is covered in more detail here. As such, developments of its mathematical and computer simulation models, SM capacitor and arm inductor design are also included.

2.1.1 Common VSC Topologies

This section will briefly outline the most common 2L and multilevel VSC topologies used in industry including the:

- Full Bridge (FB) converter
- Neutral Point Clamp (NPC) converter
- Flying Capacitor Converter (FCC)
- Cascade H-Bridge (CHB) converter
- Modular Multilevel Converter (MMC)

The Full Bridge (FB) converter is the oldest and most widely used power electronic converter for low voltage applications (<1 kV) [47] allowing rectification or inversion of AC and DC voltages. The FB converter is composed of three legs with two switches in each as shown in Fig. 2.1.

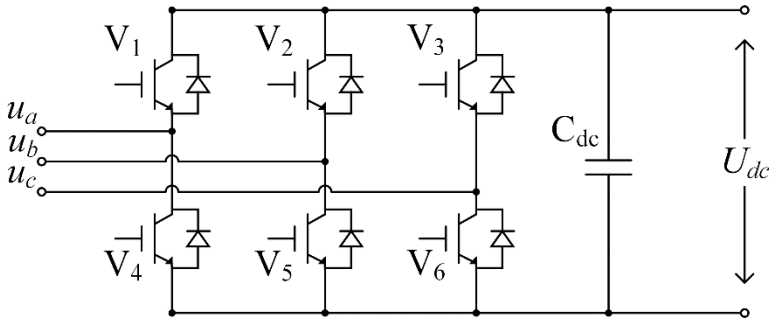


Fig. 2.1 A 3-phase 2L circuit diagram of a full bridge converter

Each leg therefore can generate a 2L AC waveform and hence creates 6 pulses per AC cycle resulting in the dominant harmonic presenting at 6 times the reference operating frequency (f_0). Using (2.1), the Total Harmonic Distortion (*THD*) can be calculated as 48 %, much higher than the Energy Networks Association's recommendation of 3 – 5% [48].

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} y_h^2}}{y_1} \tag{2.1}$$

The FB converter is therefore frequently operated with Pulse Width Modulation (PWM). This increases the dominant voltage harmonics by the multiple of the carrier frequency (f_{cr}) and hence reduces the filter size and THD of the current. The switching frequency is increased though, reducing efficiency.

Multilevel converters such as the NPC, FCC, CHB and MMC reduce the generated *THD* by creating more voltage levels. The first multilevel converter was the NPC, coming to the market in the 1980s in 3L form [49], [50]. To generate *n* levels the NPC requires *s* switches in each arm as shown in Fig. 2.2, where *s* is given by:

$$s = n - 1 \tag{2.2}$$

The DC bus is split by $n - 1$ capacitors to create clamping points which can be connected in turn to the AC terminal by the $n - 2$ clamping diodes. For a 5L NPC converter, is achieved by turning the arm switches on or off according to the switching pattern shown in Fig. 2.3. The voltage stress exhibited by the clamping diodes (u_D) is not uniform but increases towards $D_{p(s-1)}$ according to:

$$u_{D(i_s)} = \frac{U_{dc}}{(n-1)} i_s \qquad 1{:}\, i_s{:}\, s-1 \tag{2.3}$$

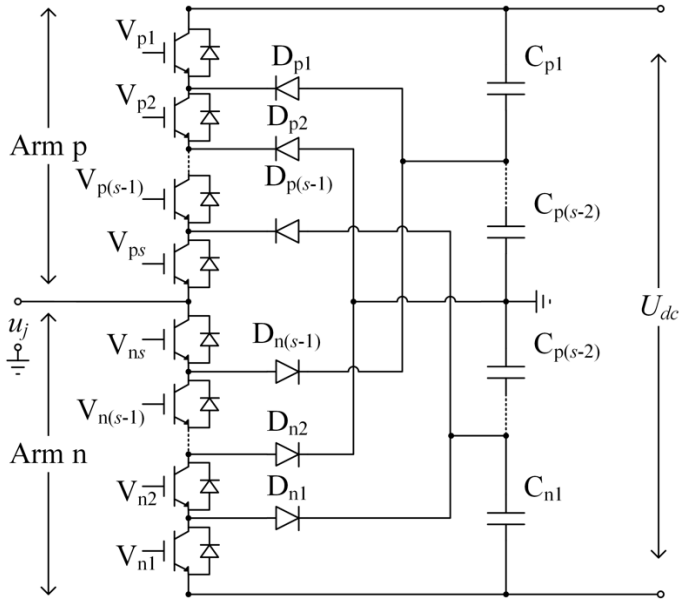


Fig. 2.2 A single-phase *n*L circuit diagram of a NPC

Therefore, above 3Ls, multiple diodes must be connected in series and the number of diodes per arm (N_D) is given by:

$$N_D = \frac{1}{2}(n-1)(n-2) \tag{2.4}$$

Additionally, above 5Ls, maintaining a stable DC capacitor voltage becomes challenging under certain operating conditions. Therefore, without changes to the standard topology, the NPC is limited to 5L [51], [52].

Valve	u_j	Logic								
	[V]	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8
1p	$U_{dc}/4$	0	0	1	0	0	0	0	0	0
2p	$U_{dc}/4$	0	1	1	1	0	0	0	0	0
3p	$U_{dc}/4$	1	1	1	1	1	0	0	0	1
4p	$U_{dc}/4$	1	1	1	1	1	1	0	1	1
4n	$U_{dc}/4$	1	1	0	1	1	1	1	1	1
3n	$U_{dc}/4$	1	0	0	0	1	1	1	1	1
2n	$U_{dc}/4$	0	0	0	0	0	1	1	1	0
1n	$U_{dc}/4$	0	0	0	0	0	0	1	1	0

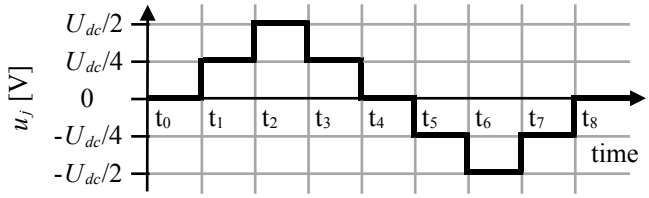


Fig. 2.3 Switching strategy for a single-phase of a 5L NPC converter

The FCC was first introduced for low power drives in the 1990's by Maynard and Foch [53] and found applications in higher power systems [54]. Unlike the NPC, multiple switching combinations can achieve the same AC voltage output. This is illustrated by comparing t_1 and t_3 or t_0 and t_4 in Fig. 2.5 where the redundant states are highlighted in green. This redundancy allows the capacitor voltages to be controlled, a significant advantage over the NPC. As can be seen in the *n*L FCC shown in Fig. 2.4, the number of switches required per arm is also given by (2.2).

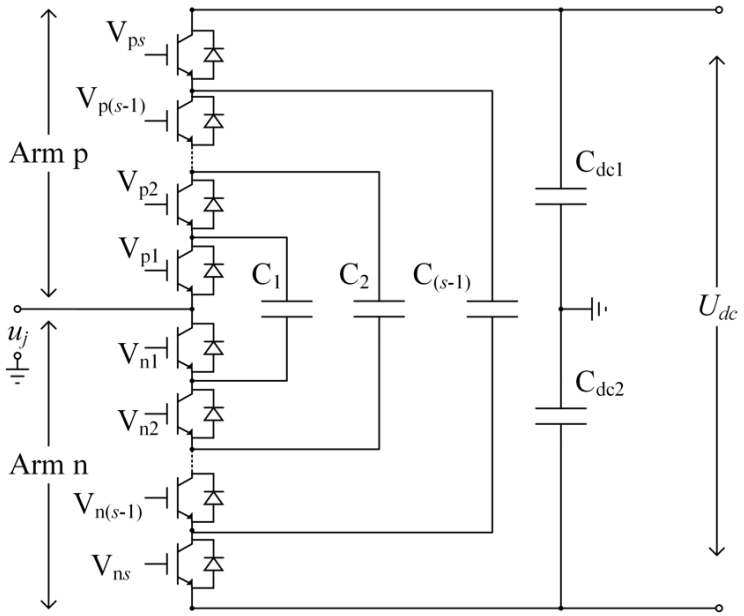


Fig. 2.4 A single-phase *n*L circuit diagram of a FCC

Like the diodes in the NPC, the capacitor voltages in the FCC also have a non-uniform distribution, such that the voltage stress increases towards $C_{s\text{-}1}$. As the voltage stress increases, multiple capacitors must be connected in series, giving the number of capacitors per branch as:

$$N_{cap} = \frac{1}{2}(n-1)(n-2) \tag{2.5}$$

Consequently, the circuit complexity increases with respect to the number of voltage levels, limiting the FCC to 5Ls in practice. While the FCC was initially considered for HVDC transmission it was rejected [54] due to its high operational losses, capacitor cost and limited voltage level creation. To reduce the capacitor size and cost, the FCC is primarily used in industrial drives where it can be operated at frequencies in excess of 1 kHz [55].

Valve	u_j [V]	Logic								
		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8
4p	$U_{dc}/4$	1	1	1	1	1	0	0	1	0
3p	$U_{dc}/4$	1	1	1	0	0	0	0	0	1
2p	$U_{dc}/4$	0	1	1	1	1	1	0	0	0
1p	$U_{dc}/4$	0	0	1	1	0	0	0	0	1
1n	$U_{dc}/4$	1	1	0	0	0	1	1	1	0
2n	$U_{dc}/4$	1	0	0	1	1	1	1	1	1
3n	$U_{dc}/4$	0	0	0	0	0	0	1	1	0
4n	$U_{dc}/4$	0	0	0	0	1	1	1	0	1

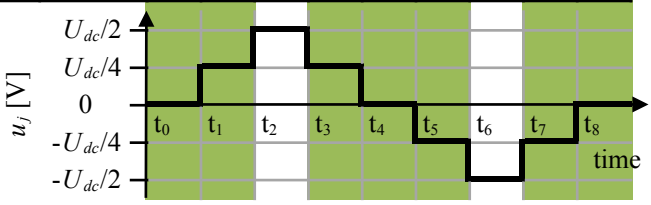


Fig. 2.5 Switching strategy for a single-phase of a 5L FCC converter

The Cascade H-Bridge (CHB) is composed of series connected H-Bridge (HB) modules within each phase or branch as shown in Fig. 2.6.

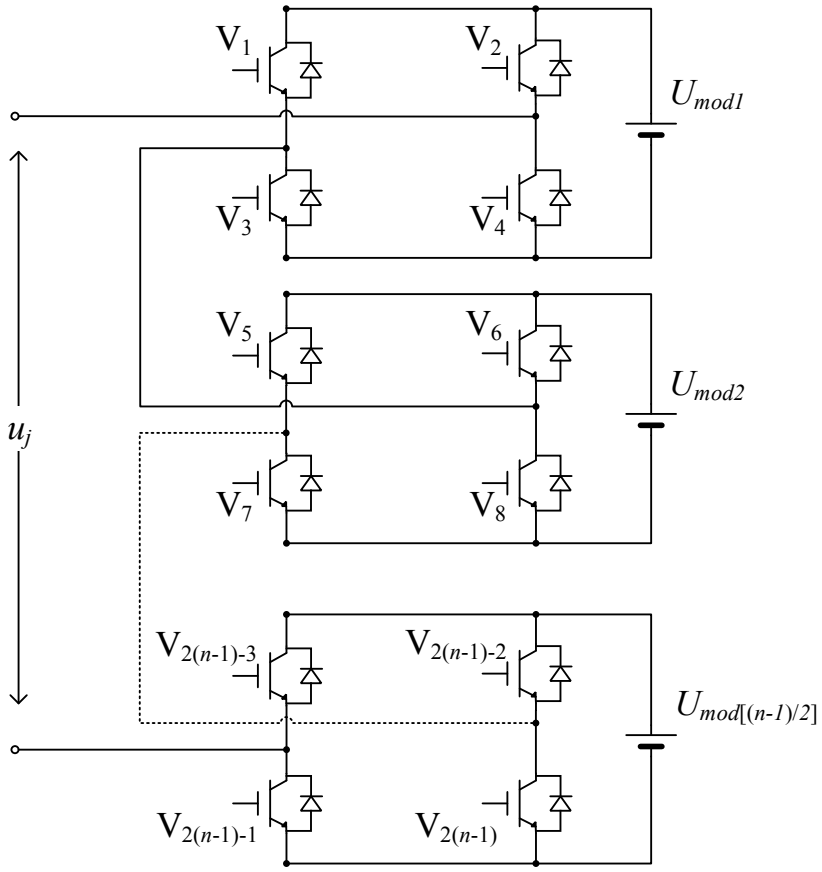


Fig. 2.6 A single-phase *n*L circuit diagram of a CHB converter

This inherent modularity simplifies the CHB design at higher numbers of voltage levels. Each module can create an output voltage of $-U_{mod}$, 0 or U_{mod} depending on the model switch states, where U_{mod} is given by:

$$U_{mod} = \frac{2U_{dc}}{n-1} \tag{2.6}$$

In addition to its modularity, the CHB also has fewer components than the NPC and FCC, as the clamping diodes and flying capacitors are not required [56] (Table 2.1). Half the number of switches required per branch is given by:

$$s = n - 1 \tag{2.7}$$

However, each module requires an isolated DC voltage source provided, either by multiple DC buses, as would be possible in a STATCOM or a Back to Back (B2B) converter or via a multi-winding transformer for transmission [55], [57], [58]. This has limited its applicability for the HVDC transmission industry as multi-winding transformers are heavy, expensive and complicated to manufacture.

Introduced by Marquardt in 2001 [59], the MMC now represents the industry standard VSC topology for HVDC applications due to the high number of voltage levels that can be created [60]. ABB have integrated it into their HVDC Light range, using press-pack Insulated Gate Bipolar Transistors (IGBT) [31], [61], [62], while Siemens use it in their HVDC Plus range [63], [64]. Alstom use a slight variation on the MMC topology to improve the efficiency of their MaxSine technology [65].

As shown in Fig. 2.7, each arm of the Half Bridge MMC (from here forward referred to as the C-MMC) consists of $m = n - 1$ SMs each containing two switch valves (V_p and V_s) and a SM capacitor (C_{mod}). Here, each valve contains n switches (S_w) in series to support the required valve voltage stress with a bypass switch (S_b) in parallel which triggers on in the case where any S_w fails. Each arm also has an inductor (L_0) to manage any circulating currents and fault currents. Other variations of the MMC topology are dealt with in [54] and analysed in detail in [32] but are not discussed further here.

Each SM can generate two voltage states, 0 V or u_c, where u_c is given by:

$$u_c = \frac{U_{dc}}{(n-1)} \tag{2.8}$$

by inserting a SM into the current path (V_s on, V_p off) or removing it (V_p off, V_s on). An example switching strategy for a 5L MMC is shown in Fig. 2.8, with the redundant states highlighted in green.

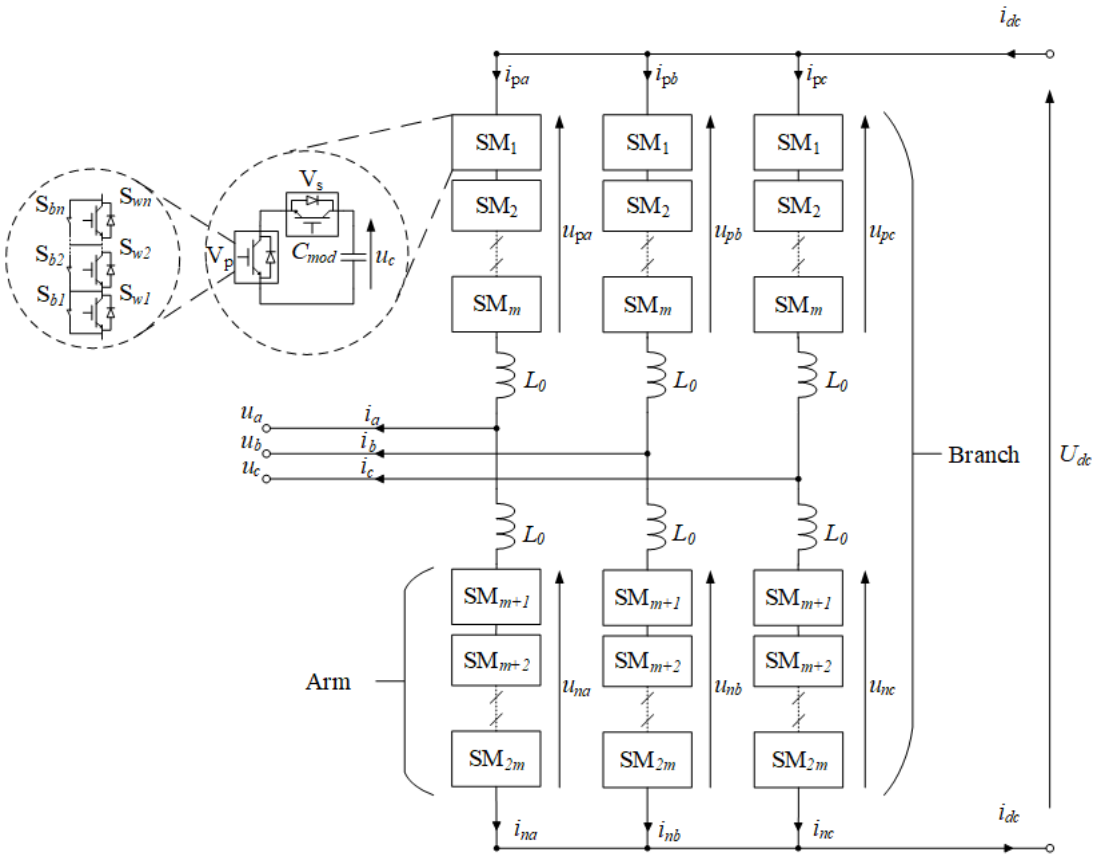


Fig. 2.7 A 3-phase Half Bridge MMC circuit diagram

SM	u_c [V]	Logic								
		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8
1	$U_{dc}/4$	0	0	0	1	1	1	1	0	0
2	$U_{dc}/4$	0	0	0	0	1	1	1	1	0
3	$U_{dc}/4$	1	0	0	0	0	1	1	1	1
4	$U_{dc}/4$	1	1	0	0	0	0	1	1	1
5	$U_{dc}/4$	1	1	1	0	0	0	0	1	1
6	$U_{dc}/4$	1	1	1	1	0	0	0	0	1
7	$U_{dc}/4$	0	1	1	1	1	0	0	0	0
8	$U_{dc}/4$	0	0	1	1	1	1	0	0	0

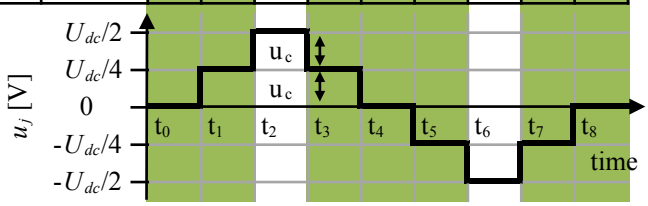


Fig. 2.8 An example switching pattern for a 5L MMC with corresponding AC waveform , redundant states highlighted

At every point, there are $n-1$ SMs on in each branch (Fig. 2.8), to support the DC bus voltage such that:

$$U_{dc} = u_{jp} + u_{jn} \tag{2.9}$$

where u_{pj} and u_{nj} are the positive and negative arm voltages of the j^{th} phase respectively. Unlike the FCC, the number of switches and capacitors required both increase linearly with the number of voltage levels as shown:

$$s = 2(n-1) \tag{2.10}$$

$$N_{cap} = (n-1) \tag{2.11}$$

While there are twice the number of switches compared to other multilevel converters (Table 2.1) it should be noted that only half are conducting at any point in time. Moreover, in a well-designed converter, these will only carry half the phase current.

Type	Valves/Branch	Switch Voltage Rating	Diodes/Branch	Capacitor or DC Source/Branch	Voltage Levels	*THD*
FB	2	U_{dc}	n/a	n/a	2L	48 %
NPC	$2(n-1)$	$\frac{U_{dc}}{n-1}$	$\frac{1}{2}(n-1)(n-2)$	$n-1$	3 – 5L	30 – 17 %
FCC	$2(n-1)$	$\frac{U_{dc}}{n-1}$	n/a	$\frac{1}{2}(n-1)(n-2)$	3 – 5L	30 – 17 %
CHB	$2(n-1)$	$\frac{2U_{dc}}{(n-1)}$	n/a	$\frac{1}{2}(n-1)$	3 – 5L	30 – 17 %
MMC	$4(n-1)$	$\frac{U_{dc}}{n-1}$	n/a	$2(n-1)$	3 – *n*L	30 – <1 %

Table 2.1 Summary of key parameters of common VSC topologies

2.1.2 Modulation Strategies for Multilevel Converters

From Table 2.1, the *THD* for most multilevel converters is still greater than the 3 – 5% recommended by [48] for grid connection. Many modulation methods exist in the literature to lower the *THD* but they also have another purpose. In the FCC and MMC, they help balance the capacitor voltages. Taking the MMC as an example, when a SM is switched into the current path, the SM capacitor will either charge or discharge depending on the polarity of the arm current (i_{arm}) where i_{arm} can represent i_{pa}, i_{na}, i_{pb}, i_{nb}, i_{pc}, i_{nc} from Fig. 2.7. When the SM is switched out of the current path its charge is preserved. It is important to ensure each SM voltage remains close to its nominal voltage to maintain consistent voltage step heights. This minimises the circulating currents generated because of differences in the state of charge between the upper and lower SMs.

Therefore, the modulation strategies commonly used in multilevel converters will be assessed on their efficiency, reduction in *THD* and capacitor voltage ripple management. The modulation strategies assessed can be broadly grouped into three categories:

- Space Vector Modulation (SVM)
- Carrier PWM (C-PWM)
- Nearest Level Modulation (NLM)

Historically SVM has been challenging to implement for *n*L converters as there was no generic control strategy [66]. As the number of voltage levels increases, the complexity and computational power required also increased and so proved unpopular. Recent research has pursued simplified [66] and generic [67], [68] SVM multi-level algorithms that aim to reduce the computation power required for higher voltage level numbers. Similar strategies can be used in MMCs after accounting for its different configuration and operation [69]. These techniques are still immature and complex to implement [70] however. In [71], NLM was found to be computationally less intensive than SVM in MMCs with many SMs while C-PWM was recommended for applications with fewer SMs. Therefore, only C-PWM and NLM are considered further.

There are several different types of C-PWM including:

- Phase Disposition (PD), Fig. 2.9a
- Phase Opposite Disposition (POD) Fig. 2.9b
- Alternative Phase Opposite Disposition (APOD) Fig. 2.9c
- Sawtooth carrier Fig. 2.9d
- Phase Shifted Carrier Fig. 2.9e

As can be seen in Fig. 2.9, each method has $N_c = n - 1$ carrier waves. In the PD, POD and APOD methods, the carrier waves have the same frequency and amplitude (A) however, they are displaced vertically such that the carrier for the i_m^{th} SM has a different initial voltage ($u_{c_{0,i_m}}$) according to (2.12).

$$u_{c_{0,i_m}} = A(m-1) - 1 \tag{2.12}$$

Where $A = 1/N_c$. The sawtooth and PSC have the same frequency and magnitude but the phase of the i_m^{th} SM waveform is phase shifted by ϕ_m.

$$\phi_m = \frac{2\pi}{N_c} \tag{2.13}$$

When PD, POD or APOD are used in a MMC topology, each SM is assigned a carrier wave. Without intervention, this leads to a high capacitor voltage ripple and very poor *THD*, [72].

This can be improved through carrier rotation techniques [73]–[76] but even so, the *THD* remains higher than sawtooth and PSC methods [72]. The switching frequency of the PSC and sawtooth methods are much higher though (Fig. 2.9), which leads to increased losses. When hundreds of SMs are used, the difference between ϕ_m and ϕ_{m+1} is small, requiring accurate carrier wave generation [77].

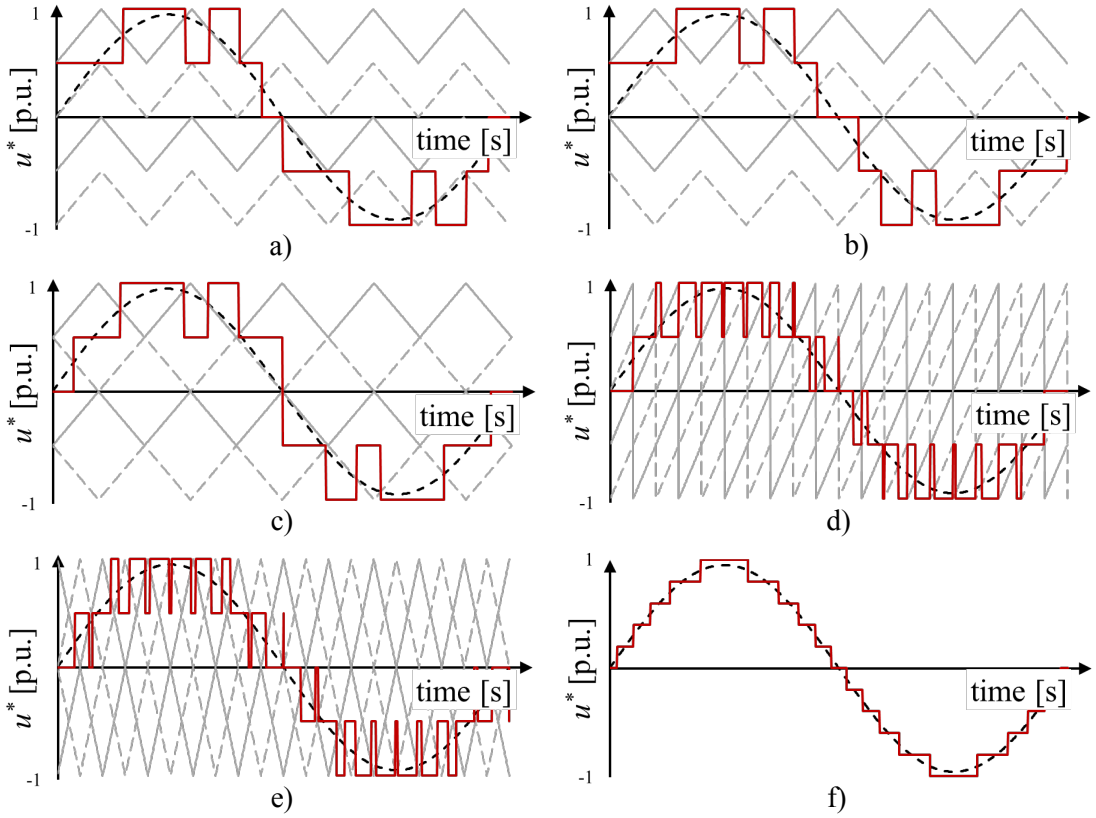


Fig. 2.9 Modulated waveforms for multilevel converters: a) PD, b) POD, c) APOD, d) Sawtooth, e) PSC and f) NLM where the PWM carriers are grey, the reference is black and the resulting AC waveform shape is red.

The NLM method does not require carrier waves but rather ensures that the average between two voltage levels traces that of the reference waveform. Therefore, it is highly suited to MMCs where *m* is large [78]. The reference and resulting AC waveform for NLM is shown in Fig. 2.9 with the number of SMs inserted in the upper arm given by:

$$\eta_{max} = round\left[\frac{1}{2}M\left(1 - u_{ref}\right)\right] \tag{2.14}$$

Variations on the NLM method have been proposed in [79], [80], where one SM operates under PWM while the rest switch at line frequency, reducing the *THD*. The PWM SM is subjected to higher switching stresses though, reducing life expectancy. In [33], [35], [78], [81] the *THD* is improved by increasing the number of voltage levels generated to $2m + 1$ by

applying a phase shift to the upper and lower arm voltages. An additional circulating current is also generated through the voltage potential setup across arm inductors. Similar approaches have been explored for C-PWM [35], [82], [83] and SVM [69] however, they exhibit the same shortcoming. The modulation strategies covered in this section are summarised in Table 2.2 where they are given a rating of 1 to 5 where 5 is the best score. The same ranking structure is used throughout this thesis.

Method	Losses	Voltage ripple	*THD*
SVM	2	5	4
SVM +	1.5	4.5	4.5
PD	4	3	2
POD	4	3	2
APOD	4	3	2
Sawtooth	2	5	3
PSC	2	5	4
PSC +	1.5	4.5	4.5
NLM	5	2	1
NLM LMS	3	3	4
NLM+	5	1	3

Table 2.2 Summary of modulation methods

The sawtooth, PSC and NLM strategies are normally coupled with a SM balancing algorithm to ensure the capacitor voltages remain balanced. These algorithms utilise the redundancies highlighted in Fig. 2.4 and Fig. 2.8 for the FCC and MMC respectively. The number of SMs that must be switched in the current path (η_m) is known from the modulation control. The algorithm then inserts the lowest η_m voltage SMs into the current path when $i_{arm} > 0$ and highest when $i_{arm} < 0$ (where i_{arm} is a generic term for the MMC arm current) as summarised in Fig. 2.10. The capacitor voltage ripple is minimised using this approach, however, it results in a very high switching frequency.

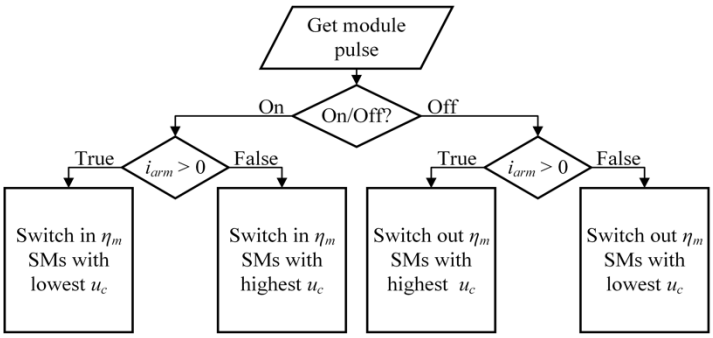


Fig. 2.10 Flow diagram of the max deviation SM balancing algorithm that designed to minimise voltage ripple

Reduced switching frequency algorithms (Fig. 2.11) have therefore been proposed in [52], [84], [85].

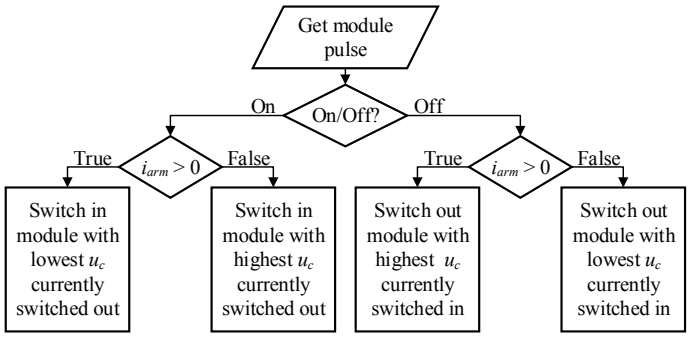


Fig. 2.11 Flow diagram of the reduced switching frequency SM balancing algorithm designed to minimise switching losses

2.1.3 MMC Design

As discussed in Section 1.4, a significant contribution of this work concerns the development and analysis of a novel MMC control algorithm. The MMC is therefore covered in more detail in this section, including the development of mathematical and simulation models and component design.

2.1.3.1 Mathematical Model of the MMC

The Thévenin equivalent circuit of the MMC, shown in Fig. 2.12, can be created assuming that there are sufficient SMs, such that they can be replaced by sinusoidal voltage sources (u_{pj} and u_{nj}). The arm resistance (R_0) represents the combined resistances of the SMs.

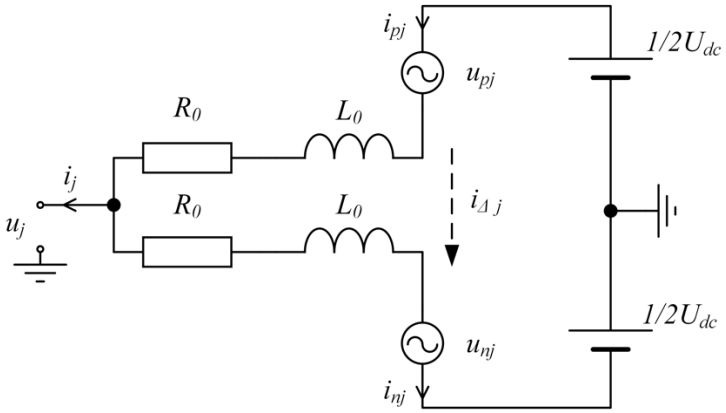


Fig. 2.12 Single-phase simplified MMC circuit diagram

It is then possible to derive expressions for the upper and lower arm currents (i_{pj} and i_{nj}) of the j^{th} phase in terms of the AC terminal current, i_j and a difference current $i_{\Delta j}$. This difference current is a circulating current that flows through the converter arms but does not appear on the AC or DC terminals.

$$i_{pj} = i_{\Delta j} + \frac{1}{2} i_j \tag{2.15}$$

$$i_{nj} = i_{\Delta j} - \frac{1}{2} i_j \tag{2.16}$$

Where:

$$i_{\Delta j} = \frac{i_{pj} + i_{nj}}{2} \tag{2.17}$$

The AC terminal voltage, u_j can also be derived from Fig. 2.12 as follows:

$$u_j = \frac{U_{dc}}{2} - R_0 i_{pj} - L_0 \frac{di_{pj}}{dt} - u_{pj} \tag{2.18}$$

$$u_j = -\frac{U_{dc}}{2} + R_0 i_{nj} + L_0 \frac{di_{nj}}{dt} + u_{nj} \tag{2.19}$$

If equations (2.15) to (2.17) are inserted into a summation of (2.18) and (2.19) it is possible to derive an expression for the output current as follows:

$$2u_j = \frac{U_{dc}}{2} - \frac{U_{dc}}{2} + (i_{nj} - i_{pj}) + L_0 \frac{d}{dt}(i_{nj} - i_{pj}) - u_{pj} + u_{nj} \tag{2.20}$$

$$2u_j = R_0(i_{\Delta j} - \frac{1}{2} i_j - i_{\Delta j} - \frac{1}{2} i_j) + L_0 \frac{d}{dt}(i_{\Delta j} - \frac{1}{2} i_j - i_{\Delta j} - \frac{1}{2} i_j) - u_{pj} + u_{nj} \tag{2.21}$$

$$e_j - \frac{R_0}{2} i_j - \frac{L_0}{2} \frac{di_j}{dt} = u_j \tag{2.22}$$

Where:

$$e_j = \frac{u_{nj} - u_{pj}}{2} \tag{2.23}$$

Similarly, if (2.19) is subtracted from (2.18) and equations (2.15) to (2.17) are inserted then it is possible to get an expression relating the difference current circulating through the arms to arm voltages.

$$\frac{U_{dc}}{2} + \frac{U_{dc}}{2} - R_0(i_{pj} + i_{nj}) - L_0 \frac{d}{dt}(i_{pj} + i_{nj}) - u_{pj} - u_{nj} = 0 \tag{2.24}$$

$$U_{dc} - 2R_0 i_{\Delta j} - 2L_0 \frac{di_{\Delta j}}{dt} - u_{pj} - u_{nj} = 0 \tag{2.25}$$

$$\frac{U_{dc}}{2} - \frac{u_{pj} + u_{nj}}{2} = R_0 i_{\Delta j} + L_0 \frac{di_{\Delta j}}{dt} \tag{2.26}$$

Then, by converting (2.22) and (2.26) to the rotating dq0 frame, robust power and circulating current controllers (CCS) can be developed [85], [86]. Their derivation is briefly covered in Section 2.1.3.2 and expanded upon in Appendix B.

2.1.3.2 Outer Converter Control

It can be seen from (2.22) that:

- The voltage on the AC terminal is solely dependent on the terminal current and the difference between the voltage sources u_{nj} and u_{pj}.
- The difference between the voltage sources creates an AC voltage within the converter with the arm inductance and resistance creating a specified arm impedance to drive the current.
- If it is assumed that the grid fixes the AC terminal voltage, then e_j can be used to control the output current.

Therefore, the inner current of the converter can be controlled simply by controlling e_j and standard dq0 control methods used by other VSCs can be employed. Using the sine oriented Parks transform, (2.22) it can be transformed to the rotating dq0 frame as shown in Appendix B to give:

$$u_d = e_d - \frac{R_0}{2} i_d + \frac{L_0}{2} i_q \omega_0 - \frac{L_0}{2} \frac{d}{dt}(i_d) \tag{2.27}$$

$$u_q = e_q - \frac{R_0}{2} i_q - \frac{L_0}{2} i_d \omega_0 - \frac{L_0}{2} \frac{d}{dt}(i_q) \tag{2.28}$$

Where d and q represent the direct and quadrature components respectively. The zeroth component sums to zero since it is assumed the *abc* phases are balanced and so is not shown. From (2.27) & (2.28), expressions (2.29) & (2.30) can then be derived for a PI based current control loop, where K_p and K_i are the proportional and integral control constants respectively.

$$e_d = u_d - \frac{L_0}{2} \omega_0 i_q - \left[K_{p1}(i_d^* - i_d) + K_{i1} \int (i_d^* - i_d) dt \right] \tag{2.29}$$

$$e_q = u_q + \frac{L_0}{2} \omega_0 i_d - \left[K_{p2}(i_q^* - i_q) + K_{i2} \int (i_q^* - i_q) dt \right] \tag{2.30}$$

The current control receives its reference currents (i_d^*, i_q^*) from the power controller which is derived from the knowledge that:

$$P = \frac{3}{2} i_d u_d \tag{2.31}$$

$$Q = -\frac{3}{2} i_q u_d \tag{2.32}$$

Therefore, an algorithm to determine the reference for the inner current controller can be derived as follows:

$$i_d^* = \frac{2}{3}P^* + K_{p3}(P^* - P) + K_{i3}\int (P^* - P)dt \tag{2.33}$$

$$i_q^* = -\frac{2}{3}Q^* + K_{p4}(Q - Q^*) + K_{i4}\int (Q - Q^*)dt \tag{2.34}$$

Where the reference real and reactive powers (P^*, Q^*) are user defined. The power controller can also be used to regulate U_{dc} in place of P if (2.33) is replaced by:

$$i_d^* = K_{p3}(U_{dc}^* - U_{dc}) + K_{i3}\int (U_{dc}^* - U_{dc})dt \tag{2.35}$$

By using the outer current control to set the reference current and monitoring and controlling the inner current directly, a faster, more responsive control algorithm is created.

Finally, an expression for a CCS controller can be derived from (2.26), since the difference current does not depend on the AC terminal voltage but only the DC bus voltage and sum of the arm voltage sources. As is shown in Appendix C, this allows the $2f_0$ circulating current (i_Δ) to be represented as a difference voltage (u_Δ). If converted into the *dq0* frame, it is then possible to drive the expressions shown in (2.36) & (2.37) to eliminate the second harmonic circulating current.

$$u_{\Delta d} = L_0 s i_{\Delta d} - 2\omega_0 L_0 i_{\Delta q} \tag{2.36}$$

$$u_{\Delta q} = L_0 s i_{\Delta q} + 2\omega_0 L_0 i_{\Delta d} \tag{2.37}$$

The final outer converter control structure is then shown in Fig. 2.9, where

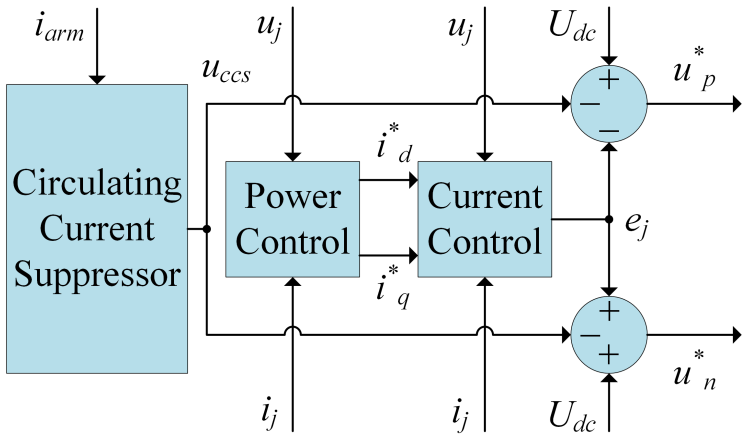


Fig. 2.13 Block diagram showing structure of the used MMC control

2.1.3.3 MMC Computer Modelling

High fidelity models of the MMC, where each SM is modelled, a large computational burden on simulation software, particularly for MMCs with many SMs. To efficiently simulate these circuits, simplified or averaged models are required. These can be grouped as follows:

- Circuit complexity reduction
- Controlled voltage source
- Analytical

The respective advantages and disadvantages and relative accuracies are discussed in detail in [87] and are briefly mentioned here and summarised in Table 2.3. In the circuit complexity reduction method, Thévenin's theorem is used to reduce the complexity of the admittance matrix created by the simulation software [88].

There are three types of controlled voltage source models, explicit SM, single equivalent SM and averaged but all use a controlled voltage source to simulate the action of the SMs as in Fig. 2.12. The explicit controlled voltage source models each SM individually, while in the single equivalent model, the SM voltages are assumed to be perfectly balanced with the same voltage and hence can be modelled as a single voltage source. The averaged model is very similar to the single equivalent model; however, it only has continuous control inputs and hence no modulation techniques can be used.

When using analytical methods, the whole system is analysed analytically, not only the SMs. This simplifies the calculations considerably as the electrical circuit has been eliminated from the model; however, it is more complicated to set up.

Modelling Method	Computational Time	Accuracy	Set-Up Complexity	Fidelity
High Fidelity	1	5	5	5
Complexity Reduction	3	4	4	4
Controlled Voltage Source	4	4	4	3
Analytical	5	3	2	2

Table 2.3 Summary of different modelling techniques

From Table 2.3, the explicit SM controlled voltage source method was selected for the MMC simulations in this thesis as it was important to maintain the individual SM behaviour. The exact model used was adapted from [87] and is shown in Fig. 2.14.

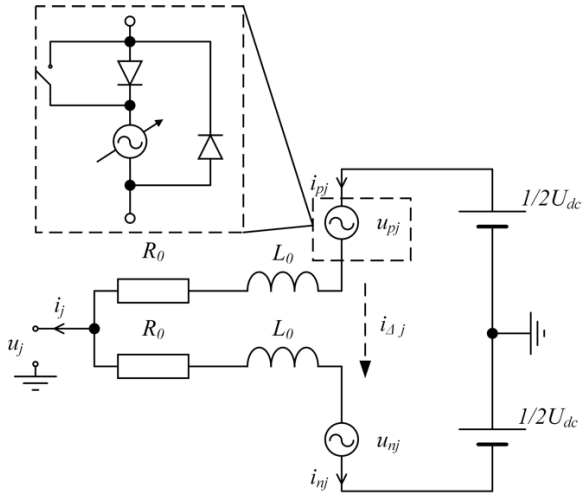


Fig. 2.14 Single-phase diagram of the explicit SM controlled voltage source model

The variable voltage source in Fig. 2.14 models the sum of the individual SM voltages (u_{cpj_z}) for the z^{th} SM in the j^{th} phase of the upper arm (p) and the individual insertion index n_{pj_z}.

$$u_{pj} = \sum_{z=1}^{m} n_{pj\_z} \cdot u_{cpj\_z} \tag{2.38}$$

The individual SM voltages can be calculated from:

$$u_{cpj\_z} = \frac{1}{C_{mod}} \int_0^t (n_{pj\_Z} \cdot \ i_{pj})\, dt \tag{2.39}$$

and the individual SM currents are given by:

$$i_{pj\_z} = n_{pj\_z} \cdot \ i_{pj} \tag{2.40}$$

2.1.3.4 SM Capacitor Design

It is known that the capacitor uses around 50% [32], [89] of the total SM volume in a standard 50 Hz MMC and so should be appropriately sized to minimise converter volume. In [90], an energy power EP ratio is introduced which for most applications is in the range of 10 ≤ EP ≤ 50 J/kVA. This provides a very simple method to estimate C_{mod} using (2.41) but is only valid for operation at 50 Hz.

$$C_{mod} = mEP\frac{S}{3U_{dc}^2} \tag{2.41}$$

A general expression to calculate C_{mod} is developed in [32] by relating the arm energy (E_{arm}) to the SM capacitance.

$$E_{arm} = \frac{1}{2} mC_{mod} u_c^2(t) \tag{2.42}$$

Inserting terms for the percentage voltage deviation Δu from a nominal value (U_c) and the maximum and minimum energy deviation ($\Delta\hat{E}_{arm}$ and $\Delta\check{E}_{arm}$) from the initial value (E_{arm_0}) provides expressions for maximum and minimum stored energy in the arm.

$$E_{arm_0} + \Delta\hat{E}_{arm} = \frac{1}{2}mC_{mod}(U_c(1+\Delta u_c)^2) \tag{2.43}$$

$$E_{arm_0} + \Delta\check{E}_{arm} = \frac{1}{2}mC_{mod}(U_c(1-\Delta u_c)^2) \tag{2.44}$$

The difference between the maximum and minimum stored energy in the arm (ΔE_{arm}) can then be described as:

$$\Delta E_{arm} = \Delta\hat{E}_{arm} - \Delta\check{E}_{arm} \tag{2.45}$$

If (2.43) and (2.44) are then inserted into (2.45) it yields:

$$\Delta E_{arm} = \left[\frac{1}{2}mC_{mod}\left(U_c(1+\Delta u_c)\right)^2 - E_{arm_0}\right] - \left[\frac{1}{2}mU_c\left(U_c(1-\Delta u_c)\right)^2 - E_{arm_0}\right] \tag{2.46}$$

$$\Delta E_{arm} = \frac{1}{2}mC_{mod}U_c^2[(1+\Delta u_c)^2 - (1-\Delta u_c)^2] \tag{2.47}$$

$$\Delta E_{arm} = \frac{1}{2}mC_{mod}U_c^2 4\Delta u_c \tag{2.48}$$

$$C_{mod} = \frac{\Delta E_{arm}}{2mU_c^2\Delta u_c} \tag{2.49}$$

So now C_{mod} is given in terms of the energy deviation for the arm but an expression relating the capacitance to the voltage deviation is required. Therefore, an expression relating the stored energy fluctuations to the voltage ripple is required. This has been developed in [32] and is reported in detail in Appendix D to give:

$$\Delta E_{arm} = \frac{S}{3\omega_0}k_c \tag{2.50}$$

where

$$k_c = \frac{\Delta\widehat{U}_j}{4\Delta u_j}\left[\frac{\Delta u_j^2}{\Delta\widehat{U}_j^2}cos(\omega_0 t - \vartheta) + cos(\omega_0 t + \vartheta)\left(\frac{\Delta u}{\Delta\widehat{U}_j^2} - 4 + 2\frac{\Delta u_j}{\Delta\widehat{U}_j}\,sin(\omega_0 t)\right) - 2\,cos(\vartheta)\left(\frac{\Delta u_j^2}{\Delta\widehat{U}_j^2} + 2\right)\right] \tag{2.51}$$

The maximum energy deviation was found in [32] to be for reactive loads ($\theta = 90^o$) at a power factor (pf = 0.9) and reduce at higher power factors. Under these conditions k was found to be 2.44 and hence (2.49) can be rewritten as:

$$C_{mod} = \frac{2.44\,S}{6mU_c^2\Delta U_c} \tag{2.52}$$

2.1.3.5 Arm Inductor Design

The arm inductor design should accomplish the following objectives:

- Limit the circulating current
- Avoid resonance with the SM capacitors
- Constrain the rise rate of the fault current

To this end, an expression relating the arm inductance to the magnitude of the second harmonic circulating current was developed for control structures without a CCS in [91]. Most converters do have a CCS however, in which case, arm inductance can be much smaller, although it must still constrain the fault current and limit the high frequency harmonics injected by the CCS as calculated in [92]. The rated fault current rise rate for power electronics generally lies in the range of 0.1 – 1 kA/μs [54] and hence the minimum L_0 can be calculated from (2.53).

$$L_0 > U_{dc}\frac{1}{\left({di_j}/{dt}\right)_{rate}} \tag{2.53}$$

For most converter applications, this is less than the minimum L_0 required to avoid second harmonic resonance with C_{mod} [54] and so L_0 should be calculated from (2.54) which is derived in full in [93].

$$L_0 > \frac{n}{\omega_0^2 C_{mod}}\frac{2(h^2-1)+m^2h^2}{8h^2(h^2-1)} \tag{2.54}$$

2.2 Magnetic Transformer

Michael Faraday created the first transformer in 1831 using a toroidal core [94]. Since then transformers have become an indispensable part of the transmission grid, facilitating power transfer between multiple voltage levels. This allows power to be disseminated throughout the country at maximum efficiency and formed one of the main arguments for using AC over DC power.

2.2.1 Transformer Loss Mechanisms

An equivalent circuit diagram for the magnetic transformer is shown in Fig. 2.15, where the magnetic losses are represented by R_{Fe} and the magnetising reactance by X_M. The winding resistances and reactances referred to the primary side are modelled by R' and X' through use of Faraday's Law (2.55) which, relates the winding voltage (u_w) to the rate of change of flux (θ) over time (t) to the number of winding turns (N_w).

$$u_w = N_w \frac{d\theta}{dt} \tag{2.55}$$

The primary and secondary voltages and currents (u_p, u_s *and* i_p, i_s) are therefore related by the turns ratio (a) and u_s can be referred to the primary side (u'_s).

$$a = \frac{N_p}{N_s} = \frac{u_p}{u_s} = \frac{i_s}{i_p} \tag{2.56}$$

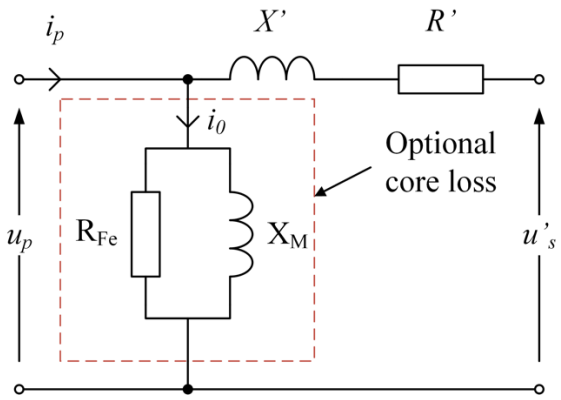


Fig. 2.15 Simplified equivalent circuit of a transformer with all impedances referred to the primary

The magnetic transformer losses are generated primarily through two mechanisms, hysteresis and eddy currents which are discussed in turn here. Hysteresis losses are generated by the changing alignment of the core material's molecules under an alternating magnetic field. This is clearly shown when the core's magnetic flux density (B) is plotted against its magnetic field strength (H) over time as in Fig. 2.16. The magneto motive force (*mmf*) is related to the line integral of H over the flux path l as well as the winding current i_w according to (2.57).

$$mmf = N_w i_w = \oint H \cdot dl \tag{2.57}$$

As H increases, the molecular structure of the ferromagnetic core becomes aligned, raising B (2.58) until the core becomes saturated. At this point the molecular structure is completely aligned and B no longer increases with H. It is therefore desirable to operate well within the linear region of the transformer, as shown in Fig. 2.16 where the BH relationship is given by:

$$H = \mu_r B \tag{2.58}$$

Where μ_r is the relative permeability of the core compared to the permeability of a vacuum (μ_0) and B is related to θ by the cross-sectional area of the core (A_c).

$$B = \frac{\theta}{A_c} \tag{2.59}$$

In an ideal transformer, the BH curve would follow the path shown by the black dotted line [0, 1, 0, 4, 0] from Fig. 2.16 as the magnetic field changes over time.

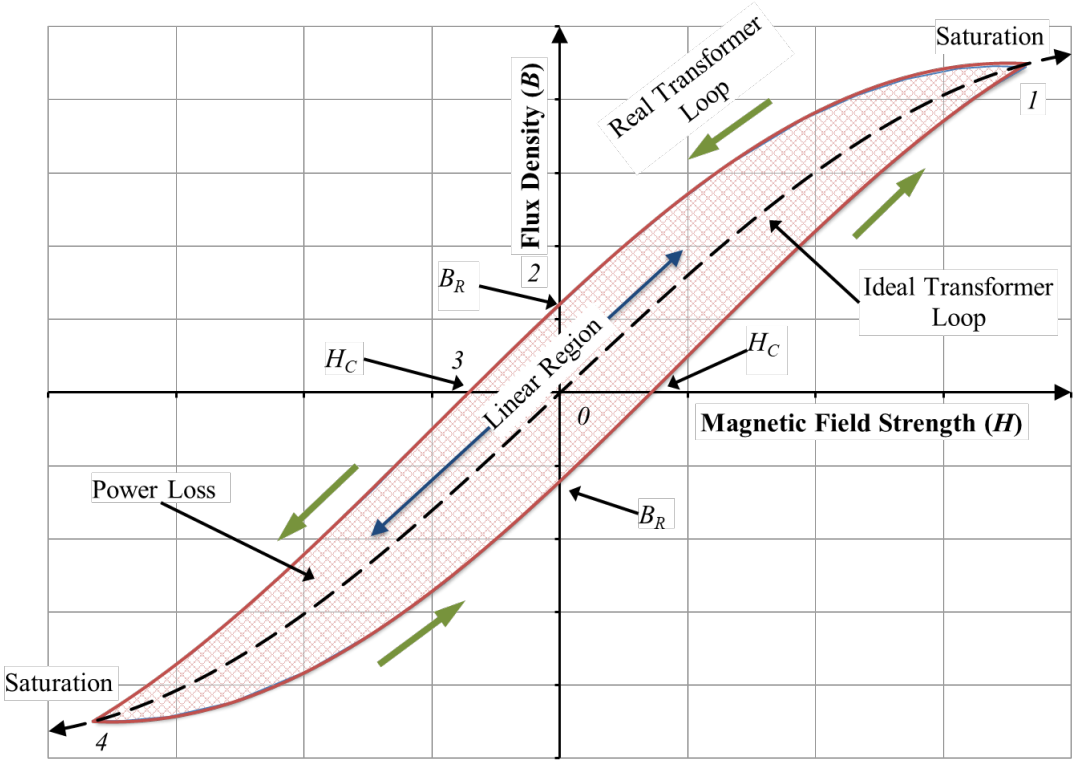


Fig. 2.16 The BH loops for an ideal and real transformer indicating the operational region, power loss (hashed region), residual magnetism and coercive force

In practice however, magnetic materials have hysteresis, as shown by the red area in Fig. 2.16. As H increases, B moves along the black dotted line from 0 to 1. As H decreases, some of the molecules remain aligned to the dissipated magnetic field and B follows the red line from 1 to 2. At this point the magnitude of B remaining in the core when $H = 0$ is called the residual magnetism (B_R). As H becomes negative, B moves from 2 to 3 before B finally returns to 0. The H required to return B to 0 is called the Coercive Force (H_c). As H continues to decrease to its minimum point B moves from 3 to 4 and then as H returns to 0, B moves along 4 to 5.

This process is repeated for each subsequent cycle and results in the anti-clockwise hysteresis loop in Fig. 2.16. The area enclosed by the loop is equal to the hysteresis loss and so by integrating the *BH* curve, the power loss (P_{hyst}) may be calculated as shown by the hashed region in Fig. 2.16.

$$P_{hyst} = f_0 \oint B \cdot dH \tag{2.60}$$

The second loss mechanism in transformer cores is known as eddy current losses (P_{ed}) and is the result of induced currents forming in the core due to the changing magnetic flux. From (2.55) it is known that a changing flux will induce an Electromotive Force (EMF), u_{lz} and hence current in the core. By applying Lenz's Law, the direction of the induced current will be such that it will induce a flux that opposes the flux that created it as shown in (2.61).

$$u_{lz} \propto -\frac{d\theta}{dt} \tag{2.61}$$

Traditionally transformer cores have been constructed of iron and so the induced EMF will create a large eddy current and hence loss. These losses can be approximated by (2.62) and shows that they are proportional to the peak flux density ($\hat{B}$), frequency, the width of the smallest perpendicular dimension of the core to the flux path (W_d) and a core shape constant (k_s), where ρ_c is the core's electrical resistivity [25].

$$P_{ed} = \frac{k_s \, \hat{B} \, 2 f_0^2 W_d}{\rho_c} \tag{2.62}$$

A common method to minimise these losses has been to form the core of many thin laminations Fig. 2.17 with an electrical insulating varnish between each layer and reducing W_d and hence P_{ed}.

This is effective at grid frequencies (50/60 Hz) but recently, higher frequency transformers have become more common. This is because transformer volume which is roughly equivalent to the transformer core (A_c) and winding area ($A_{winding}$) is inversely proportional to frequency.

$$A_{winding} A_c \propto \frac{1}{f_0} \cdot \frac{U_{rms} I_{rms}}{J \hat{B}} \tag{2.63}$$

Where *J* is winding current density. Therefore, transformer size can be greatly reduced if operated in the MF range.

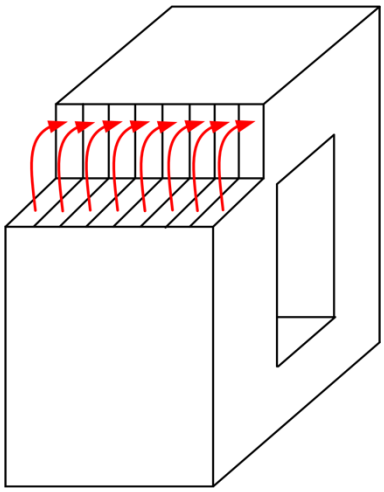


Fig. 2.17 A laminated transformer core

With the improvements in power electronics this is a realistic operating frequency for DC transformers and allows them to fully utilise the added flexibility of having a primary and secondary converter [95]. Medium Frequency Power Transformers (MFPT) are therefore highly attractive in many industries where size and weight are important such as traction systems [96] and aerospace. They are becoming increasingly investigated for offshore wind farms [97].

2.2.2 Magnetic Transformer Materials and Shapes

In the MF range magnetic losses increase significantly [29]. Core laminations are too thick to limit eddy currents and hysteresis loops too large, resulting in large hysteresis losses. New materials with a higher ρ_c and small hysteresis loops such as amorphous and nanocrystalline materials are therefore used to reduce losses. This section briefly discusses their properties and summarises their relative merits.

Ferrites, a form of ceramic, are manufactured in using a sintering process which can greatly affect the mechanical and electromagnetic properties of the material [98]. They are extensively used in high frequency transformers as they exhibit low eddy current losses, however, their saturation flux density is low [98]. Ferromagnetic metals made a comeback in the 1960/1970s [99] with the advent of amorphous metals through rapid cooling technology [100], [101]. This process prevents crystallisation, resulting in higher electrical resistivity compared with standard ferromagnetic materials and creates very thin laminations greatly reducing eddy current losses while maintaining a reasonable saturation flux density [102]. If the amorphous ribbon is reheated to 500-600^{o}C very fine iron-silicon grains are formed (10 – 15 nm) [98],

[103]. This annealing process creates a material with very low core losses but high flux densities [96], [103], [104] and as a result, is highly sought after. The properties of each core material are summarised in Table 2.4.

Material	Saturation Flux Density	Core Loss
Silicon Steel[1]	1.48 – 1.53 T	1.06 – 1.6 kW/kg
Ferrite[2]	0.38 – 0.53 T	0.017 – 0.039 kW/kg
Amorphous[1]	0.82 – 1.59 T	0.14 – 1.5 kW/kg
Nanocrystalline[1]	1.2 – 1.23 T	0.04 – 0.07 kW/kg

Table 2.4 Saturation flux densities and core losses for common transformer materials. Core losses normalised to: [1] B = 1T and @ 20 kHz and [2] B = 0.2 T @ 25 kHz [29], [105]

In addition to the core material, the core shape also plays an important role in the transformer's performance. Power transformers can either be single or 3-phase. Generally, three single-phase transformers are used for very high-power applications where a single, 3-phase unit is impractical from a logistical perspective due to its size. As each core is independent, incorporating redundancy and maintenance operations are also simplified [106], [107].

The most efficient single core shape is the toroidal core (Fig. 2.18a). Its design minimises leakage inductance, offers higher flux densities and limits Electromagnetic Interference (EMI) [94], [108], [109]. Its windings completely cover the core, limiting cooling and hence its power rating although some higher power designs are now being considered [94]. Pot cores (Fig. 2.18b) have similar attributes to toroidal cores except the windings can be wound around a bobbin, simplifying manufacture but their power ratings are generally still limited, although they are improving [108].

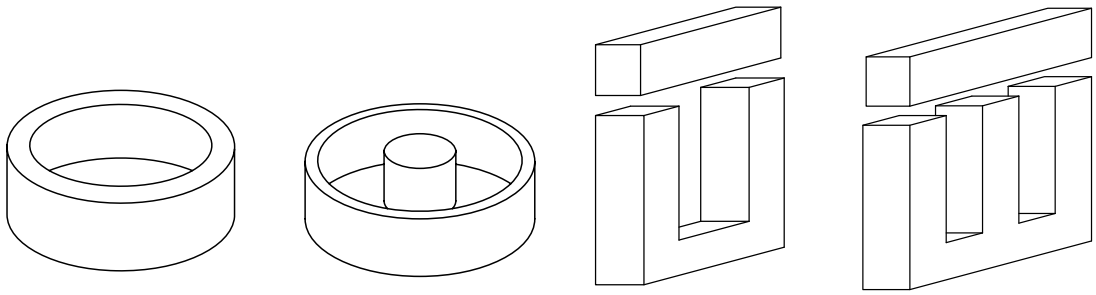


Fig. 2.18 Common transformer core designs (a) toroidal, (b) Pot, (c) U or C core, (d) E or shell, toroidal

The most common core shapes used for high power applications are the U or C (Fig. 2.18c) and E or Shell (Fig. 2.18d) cores. The U-core is more efficient and compact in single-phase than the E-core [96], [28], however, this reverses for 3-phase applications. According to (2.64), the flux components from each phase in a 3-phase transformer sums to 0 under balanced load.

The leg that would carry this flux can therefore be omitted and one phase can be wound around each leg of the E-core, less material is therefore required compared to 3 single-phase U-cores and efficiency is improved [110].

$$\theta\, sin(\omega_0 t) + \theta sin(\omega_0 t - 2\pi/3\,) + \theta sin(\omega_0 t + 2\pi/3\,) = 0 \tag{2.64}$$

A summary of each core shape discussed in terms of efficiency, maximum power rating and access for cooling, ranking each out of 5 is given in Table 2.5.

Core Type	Efficiency	Power Rating	Cooling Access
Toroidal	5	1	1
Pot	4	2	2
U or C	4	4	4
E or Shell 1: phase	2	4	5
E or Shell 3: phase	4	5	4

Table 2.5 Summary of core shapes

2.2.3 Review of Core Loss Equations

To accurately specify the transformer's thermal management and determine efficiencies an accurate calculation of core losses is critical. Traditionally, the empirical Steinmetz Equation [111] given by (2.65) was used to calculate core losses where the Steinmetz parameters, k_{SE}, α and β are material constants [112], [113], normally provided by core manufacturers.

$$P_{core} = k_{SE} f_0^{\alpha} \hat{B}^{\beta} \tag{2.65}$$

However, the SE is only valid for sine waves [36], which is a severe limitation, as the power electronics used in DC transformers produce non-sinusoidal waves. Often in such cases, the SE is used in conjunction with the FT of B. However, the non-linearity of the SE leads to inaccurate results using this approach, although the extent of this inaccuracy has not been quantified in the literature [114]. Other approaches to calculate the core loss of non-sinusoidal waveforms can be categorised into 3 groups:

- Hysteresis models
- Separation of loss components
- Empirical solutions

The most common Hysteresis method is the Jiles Atherton [37], [38], due to its low computation cost and relatively small number of parameters. It is primarily used in conjunction with simulation software. The material parameters required are not provided by manufacturers [41] but are sometimes pre-loaded in the software packages. The parameters required in the separation of loss components are also not readily available, however, due to recent works [39]–[41] to explain excess eddy currents, it has become relatively accurate. Progress has been

made to simplify the derivation of the loss components [42], [43], but they are still more time consuming than other methods.

Empirical methods are largely based on modifications of the SE and as a result the core loss is relatively simple to calculate from the parameters provided by manufacturers. One of the first of such empirical methods, the Modified Steinmetz Equation (MSE), replaced f_0 with an equivalent frequency to account for the additional harmonics [44], [45]. The General Steinmetz Equation (GSE) [46], assumed the core loss could be calculated from the instantaneous rate of change of B although often led to inaccurate results. The Improved General Steinmetz Equation (iGSE) addressed this shortcoming a year later [36] and now represents one of the most accurate and simple to use options [41]. A further addition to the iGSE is proposed in [115] to take relaxation effects into account; however, it is significantly more complex to implement.

To apply the iGSE the flux density waveform must be calculated from the input voltage using (2.55) and (2.59) and split into n_c individual cycles. The rising and falling sections of each n_c cycle must then be separated, i.e. the cycle's global minimum to maximum and global maximum to minimum respectively. If there are multiple global maxima or minima either can be chosen. An example flux density waveform is shown in Fig. 2.19. It has been split into its rising and falling sections with the minor loops in each identified in red. The black line forms the major loop of the rising and falling sections.

An algorithm then splits the waveform into its minor and major loops, calculating the power loss of each loop individually using (2.66) – (2.68).

$$k_{iGSE} = \frac{k_{SE}}{(2\pi)^{\alpha-1} \cdot 2^{\beta-\alpha} \int_0^{2\pi} |cos\vartheta|^{\alpha} d\vartheta} \tag{2.66}$$

$$p_o = \frac{1}{T_o} \int_0^{T_o} k_{iGSE} \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{2.67}$$

or, as a discrete function:

$$p_o = \frac{k_{iGSE} \Delta B^{\alpha-1}}{T_o} \sum_{i_t=1} \left|\frac{\delta B_{i_t}}{\delta t_{i_t}}\right|^{\alpha} \delta t_{i_t} \tag{2.68}$$

Total core loss is then determined by a weighted average of the power from each loop as in (2.69) and the average loss of all the cycles of the waveform calculated by applying (2.70).

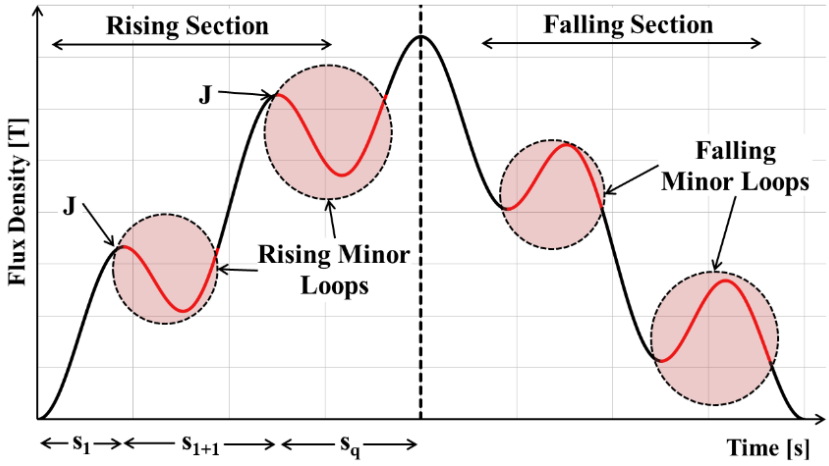


Fig. 2.19 Splitting of an example flux density waveform into its major and minor loops

$$p_{core_l} = \sum_{o=1} p_o \frac{T_o}{T_{cycle}} \tag{2.69}$$

$$P_{core} = \frac{1}{n_c} \sum_{i_l=1} p_{core_{i_l}} \tag{2.70}$$

Where p_o is the core loss for each major or minor sub loop of the l^{th} cycle, δB_i and δt_i are the change in flux and time between times step i_t and i_{t-1} and T_{cycle} and T_o are the periods of the cycle of the o^{th} loop and cycle and ϑ is the phase angle.

2.2.4 Windings

The windings form a key part of any transformer design and make a significant contribution to the efficiency, cost and volume of the design. This section discusses the main winding types available to the designer, assessing them based on their cost, space utilisation and mitigation of the key winding loss mechanisms. The equations to calculate the winding losses are also provided.

2.2.4.1 Winding Loss Mechanisms

Within the transformer windings, there are three primary loss mechanisms,

- DC resistive losses
- The skin effect
- Proximity effect

In its simplest form, the transformer winding is a length of wire and as such, has a DC resistance (R_{dc}), based on the conductor's mean length (l_w), cross sectional area (A_w) and resistivity at a given temperature.

$$R_{dc} = \frac{\rho_w l_w}{A_w} \tag{2.71}$$

At low frequencies, the winding resistance and hence loss can be accurately represented by (2.71) however, at higher frequencies mutual and self-inductance effects begin to dominate and can no longer be ignored.

From Lenz's law (2.61) and Fleming's right-hand rule, the induced current flows in the direction of primary current at the outer radius of the wire but in the opposite direction in the centre. Most of the power is therefore carried by the outer radius of the cable, this is known as the skin effect. The skin depth (δ) is calculated from:

$$\delta = \sqrt{\frac{2\rho_w}{\omega_0 \mu_r}} \tag{2.72}$$

As a rule of thumb, the skin effect in conductors can be ignored if the conductor's diameter, d_w is:

$$d_w < 2\delta \tag{2.73}$$

This clearly presents challenges for high power, high frequency transformers as the wire's power rating is normally determined by its diameter.

Further to the skin effect the electromagnetic field created by the AC currents also induces a current in neighbouring windings, termed the proximity effect. This is proportional to the frequency and the distance from the respective winding. This is not dealt with any further in this thesis as at the frequencies in question its effect is minimal.

2.2.4.2 Types of Winding

There are three main categories of windings available for use in magnetic transformer including: single core, multi-strand/litz and foil. Single core (Fig. 2.20a) is primarily used for low frequency applications as its resistance is heavily influenced by the skin effect. In multi-strand wire/litz wire (Fig. 2.20b) many insulated thin strands of wire are twisted together to mitigate the effect of the skin effect but are costly to manufacture and have a low copper density.

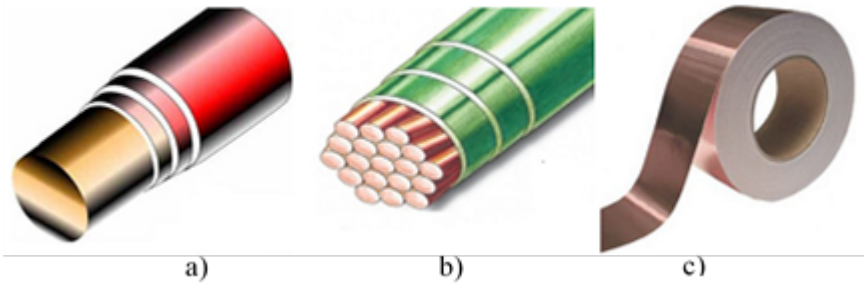


Fig. 2.20 Common transformer winding types including (a) single core, (b) multicore/litz and (c) foil [96]

Foil windings have a rectangular cross section (Fig. 2.20c), and are relatively unaffected by the skin effect and have a very high copper density. A summary of the different conductor types is given in Table 2.6

	R_{ac}/R_{dc}	Cost	Copper Density	Current/Frequency
Solid	5	2	4	2
Litz	1	4	2	5
Foil	2	2	5	4

Table 2.6 Summary of transformer winding properties

2.2.4.3 AC Resistance

From Table 2.6 transformer winding's AC resistance is dependent not only on f_0 but also on the winding type. There has therefore been much research to mathematically describe the AC resistance such that winding power losses can be accurately calculated. This section summarises the winding loss equations used in this thesis.

Dowell was the first to solve Maxwell's equations specifically for transformer windings, providing an accurate closed form equation for foil windings in 1966 [116]. This equation become known as Dowell's expression and is based on the following assumptions [117]:

- One dimensional analysis is valid for close foil conductors
- Foil conductors utilise the entire window height and the magnetic field can be represented solely in this dimension
- The magnetic core is infinitely permeable

Dowell also proposed correction factors to generalise the equation for other winding types and configurations resulting in the following equations:

$$R_{ac} = R_{dc}\Delta\left[\left(\frac{sinh(2\Delta)+sin(2\Delta)}{cosh(2\Delta)-cos(2\Delta)}\right)+\frac{2(N_w^2-1)}{3}\left(\frac{sinh(2\Delta)-sin(2\Delta)}{cosh(2\Delta)+cos(2\Delta)}\right)\right] \quad (2.74)$$

Where Δ is given by:

$$\Delta = \eta_w'' \frac{t_w}{\delta}, \qquad \eta_w'' = \eta_w' \eta_w \tag{2.75}$$

The steps required to use Dowell's generalised formula are given in detail in Appendix E. Studies show that this method provides similar results to other calculation methods for both round and square conductors [118], [119] as shown by analysis in [120], [121]. As the porosity factor increases (such as in litz wires) the accuracy of Dowell's equation does reduce [120]. Mathematical expressions to more accurately describe the AC resistance of litz wires are detailed in Appendix F.

2.3 System Analysis

2.3.1 Wind Farm Collection Systems

This section examines the overall wind farm topologies that are currently employed by industry, their limitations and the proposed solutions by both industry and academia. By analysing what has been proposed and the respective limitations, it is possible to propose a practical topology for the Hybrid HVDC transformer concept taking full advantage of its capabilities.

2.3.1.1 AC Transmission

The majority of fully operational offshore wind projects use either High (> 69 kV) or Medium (1 kV to 69 kV) [122] Voltage AC (HVAC or MVAC) cables for power transmission [123]–[127]. The wind turbines are connected to the transmission cable or AC substation by 33 kV 3-phase inter-array cables [128] as shown in Fig. 2.21, although future inter-array cables are likely to be 66 kV to reduce the wind farm costs and increase efficiency [129].

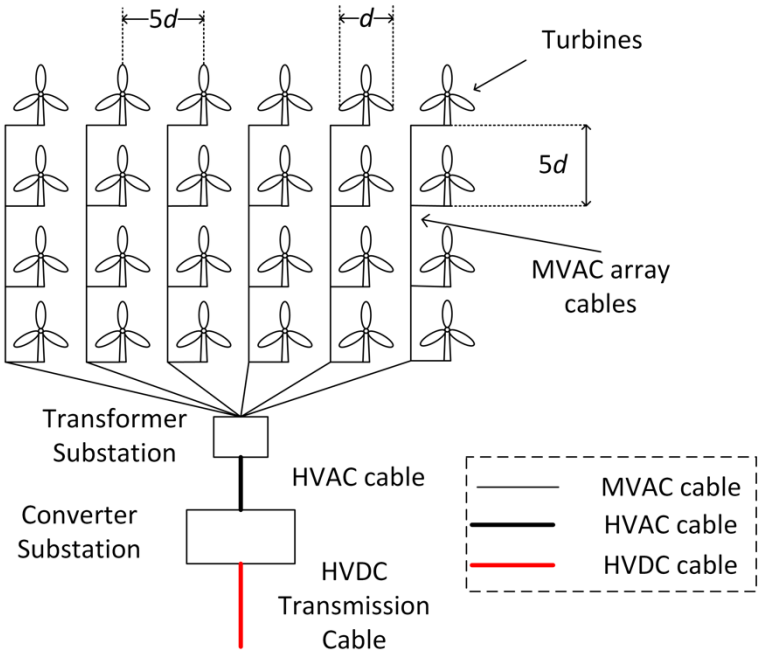


Fig. 2.21 A conventional HVAC wind farm topology

Most modern, large (> 5 MW) wind turbines have a permanent magnet synchronous generator with fully rated active back to back (B2B) converters to allow for Maximum Power Point Tracking (MPPT). A 50 Hz transformer located in either the turbine nacelle or tower then steps up the turbine voltage for connection to the inter-array grid. This has been shown ([130], [131]) to be the most cost effective solution for near shore, low power wind farms.

AC cables suffer from large parasitic losses over long distances however, reducing the active power rating of the cable [11] as shown in Fig. 1.2. To maximise the transmission distance, reactive power compensation must be supplied both on and offshore, significantly increasing costs. Consequently, there are financial and practical limitations on AC cable transmission lengths [130]–[132]. Alternative solutions will be required for longer transmission distances and larger wind farm power ratings [123]–[127].

2.3.1.2 DC Transmission

To mitigate these AC parasitic losses, wind farms far from the PCC use HVDC transmission systems. There are two HVDC systems available, Line Commutated Converter (LCC) and VSC based solutions. LCC systems have higher power ratings and are less expensive but occupy a 67% larger footprint compared to VSC systems [133], [134]. Strong grid connections at both terminals are also required. They are therefore considered unsuitable for offshore wind farms [130], where the AC inter-array grid is weak and space on the offshore platforms is

expensive. VSC systems however, can operate in weak grids [54] and offer black start capabilities and thus are suitable for offshore wind farm transmission.

Typically, one HVDC substation services multiple wind farms as shown in Fig. 2.22 via an AC transformer substation. HVDC wind farms therefore require additional expensive hardware (the HVDC substation costs >£400M [11]) irrespective of the transmission distance.

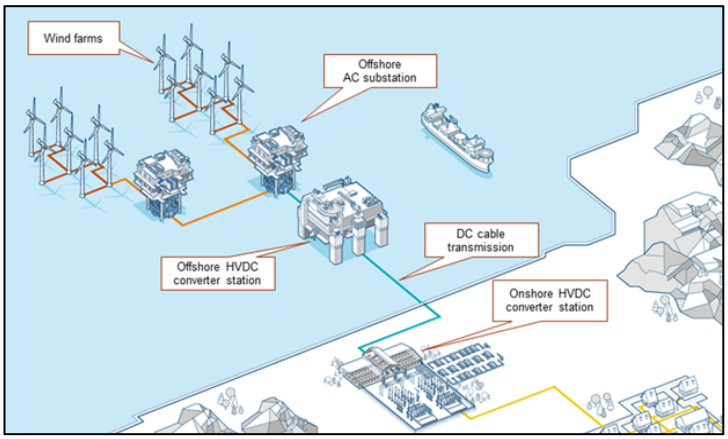


Fig. 2.22 Current HVDC collection system with AC grid [135]

It is therefore only used over long distances where the savings in cable reactive power compensation outweigh the costs of the HVDC substation, as shown in Fig. 1.3. The critical distance from Fig. 1.3 is project specific but has been decreasing. Efforts to reduce the cost of HVDC were initially restricted, as seven projects were commissioned in parallel using six different designs leaving no time to learn from mistakes [17].

Operation and Maintenance (O&M) contributes 18 – 20% of an offshore wind farm's cost of energy [136], with converters and specifically IGBTs, accounting for a significant proportion of failures [137], [138]. Much work has therefore focussed on developing more robust topologies by eliminating or replacing active components in both the turbines and substations with diodes as in [134], [139]–[143]. This would reduce the size and cost of the platform and turbine but additional harmonics would be injected and operators would have less control over turbine operation. Additionally, these topologies fail to address the lack of system redundancy in HVDC transmission systems. Presently redundancy only exists within each platform so that if a switch fails the converter would continue to function. A serious fault however, such as a fire [18], AC inter-array grid problems [19] or indeed if the platform should become damaged in a storm, would cut out power from multiple wind farms.

To cut the cost of the HVDC platform and improve redundancy, Siemens developed the DRU [21]. Here the HVDC and AC transformer substations are replaced by several DRUs. Voltage

on the DC side is increased through series connection of the DRUs which can fit on a platform similar in size to those used by existing AC transformer substations. The number and cost of the offshore substations is therefore reduced and redundancy is increased. While this does reduce the costs compared to conventional HVDC systems, the substation costs are still high as shown in Chapter 6.

If costs are to be reduced further, the offshore substations should be eliminated [144], requiring turbines to export directly to a DC grid. To minimise weight and avoid complications of MF and High Frequency (MF) transformer design, the isolating magnetic transformer can be eliminated as in [1], [2], [22]–[24] where resonant DC/DC converters are used in its place. Resonant converters generally have a narrow range of operation however and are complicated to design. Their step up ratios are also limited and often require large inductors [2] or capacitors [1], [22].

While MF isolating magnetic transformers present the opportunity to reach high step-up ratios, most are designed for relatively low voltages [25]–[30]. Two or three level converters are therefore often used allowing for zero current or zero voltage switching (ZCS or ZVS) strategies to be implemented. Challenges posed by large discrepancies between voltage and current magnitudes between the primary and secondary converters can also be omitted simplifying the converter design.

2.3.2 DC System Protection

Initially, a fault situation must be identified, i.e. an overcurrent must be recognised and then acted upon to prevent it damaging grid components. After the fault has been cleared the affected area should be re-energised.

Fault isolation is difficult to achieve in DC systems though, since there is no natural zero current crossing point [145]–[147]. A different Circuit Breaker (CB) technology is therefore required to force a zero-current condition and extinguish the electrical arc [145], [148]. Furthermore, due to the low inherent inductance in DC systems, the fault current rises quicker than in AC systems [145], [149]. Siemens and Alstom estimate that a DC fault should be isolated in less than 5 ms to avoid the system voltage collapsing [150].

There are three types of DC CB, including electromechanical, where a resonant circuit in parallel with a fast-acting mechanical switch extinguishes the arc in the event of a system trip. This provides a relatively slow isolation time (similar to AC CBs) but is very efficient [148].

In solid state CBs, the mechanical switch is replaced by a semiconductor based switch (GTO, IGBT or IGCT). This leads to very fast isolation times (100 μs) [151] however, the losses are high (30% of a HVDC substation) [150]. Hybrid CBs, use a combination of mechanical and semiconductor switches in the current path and an energy dispersion device in parallel [145], [149]. ABB, Alstom and Siemens have had success using this DC CB type achieving isolation times in the region of 2 – 5 ms [125], [152], [153]. All three DC CB are summarised in Table 2.7 below.

	Electromechanical	Solid State	Hybrid
Interrupt Time	1	5	4
Efficiency	5	1	3
Practicality	2	2	3

Table 2.7 Summary of the properties of the available CB designs

Since these CBs are still prohibitively expensive and largely untested commercially, present HVDC wind farms use AC CBs on the AC side of the converter instead. If a fault occurs in the DC transmission section, the system is allowed to discharge to clear the fault before it is re-energised [146], [149], [154]. There have been proposals to use a similar system for large HVDC networks [146], [154] however, due to the increased capacitance in the system it would take significantly longer to charge and discharge.

2.4 Chapter Conclusions

The aim of this chapter was to place Hybrid HVDC Transformer in the context of the background literature so that the remaining technical challenges and knowledge gaps could be identified. Through investigation of the objectives stated at the beginning of the chapter, several key outcomes and gaps in the literature were identified including:

- To achieve the high step ratio required for the Hybrid HVDC Transformer, a magnetic, isolating transformer is required
- The converters will generate non-sinusoidal flux waveforms in the core, complicating the calculation of core losses
- Industry and academia differ in their approach to the calculation of core losses under non-sinusoidal excitation and the difference in accuracy between each method is not adequately reported in the literature
- The magnetic DC transformer topologies presented in the literature cover relatively low step-up ratios. The analysis of these topologies therefore favoured LV converter topologies and did not consider the impact of large differences in current magnitudes between the primary and secondary converters
- The standard MMC control strategies make inefficient use of the available hardware, limiting the number of voltage levels that can be created in LV and MV applications

- Proposed methods to increase the number of voltage levels generated result in uncontrollable circulating currents or are very limited in terms of their applicable applications
- Potential cost reductions of the DRU concept have been presented but an independent economic cost reduction is required.

These gaps are covered in the later chapters as follows; an evaluation of different topologies and core loss calculation methods is conducted in Chapter 3. This reveals that the Hybrid HVDC Transformer's efficiency is highly sensitive to the converter switching frequency. A novel MMC control algorithm to generate additional voltage levels through more efficient use of the converter hardware is proposed and validated through experiment in Chapter 4. The operational range and potential improvement to the algorithm is then presented in Chapter 5. An economic analysis of the Hybrid HVDC Transformer, DRU and potential future iteration of the DRU is conducted in Chapter 6 and compared to the cost of a conventional HVDC topology. Finally, key conclusions from this work and next steps required are covered in Chapter 7.

Chapter 3 The Hybrid HVDC DC/DC Transformer

To achieve a high step-up ratio within the confined space of an offshore wind turbine, the Hybrid HVDC Transformer should be based on a MF, magnetic transformer design. This will increase the loss density of the transformer's core and windings so an accurate loss calculation is required. The trade off in accuracy in using the simpler FTSE compared to the iGSE for Ferrite cores in the MF range was identified as a knowledge area gap in Chapter 2 however. Given the importance of this calculation, the accuracy of both methods should be well defined.

Furthermore, the DC converters within the Hybrid HVDC Transformer will be subjected to large current stresses on the primary side and significant voltage stresses on the secondary due to the high step-up ratio. Previous converter studies favoured LV converter designs with ZVS or ZCS to minimise the converter switching losses. Such topologies may be unsuitable for HV applications however, and are very challenging to design.

To that end, the aim of this chapter is to characterise the accuracies of the FTSE and iGSE and determine the best topology and operating frequency for the Hybrid HVDC Transformer and hence fill in the identified knowledge gaps. The results of the FTSE and iGSE comparison will be used to inform the mathematical model design for the magnetic transformer and will be used in conjunction with a simulation model of different converter topologies. These models will be run over a range of frequencies to determine the optimum design and operating frequency.

The key objectives of the chapter can therefore be summarised as follows:

- Characterisation of the difference in accuracy between the FTSE and iGSE
- Determination of the Steinmetz parameters for the N87 Ferrite material in the 500 – 2000 Hz range

- Determination of the optimum converter topology for use in a high step-up ratio transformer
- Selection of the optimum operating frequency and magnetic transformer design
- Identification of the key loss mechanisms in the Hybrid HVDC Transformer

To accomplish these objectives, this chapter is organised as follows; the Hybrid HVDC transformer specifications are identified in Section 3.1. The experiment set-up and results of the accuracy comparison of the FTSE and iGSE are presented in Section 3.2. The mathematical model of the magnetic transformer, including the core shape and size, winding selection and loss calculations are discussed in Section 3.3. The MATLAB/Simulink converter models and loss calculations are presented in Section 3.4. The converter and magnetic transformer models are then used to calculate the efficiency and volume of each topology and operating frequency with the results presented and discussed in Section 3.5. Finally, the key conclusions are outlined in the chapter summery contained in Section 3.6.

3.1 Transformer Specifications

To ensure a fair and realistic comparison between each configuration, the transformer specifications must be held constant and should be based on current or predicted trends. This section outlines the key transformer specifications used in the analysis and the reasoning behind their use.

As the Hybrid Transformer represents a significant change from the status quo, it will most likely be integrated into the next generation of offshore wind turbines. At present, MHI Vestas have released an 9.5 MW (V164-9.5 MW) turbine although this is largely based on the 8 MW (V164-8 MW) model with Siemens widely rumoured to have an equivalent turbine in the pipeline [155]. For this reason, a 10MW turbine with fully rated power electronics for variable speed operation (as is common for modern turbines) is used for the converter comparison with the Hybrid HVDC Transformer located as is shown in Fig. 3.1. As space and weight are limited, the Hybrid Transformer will operate in the MF range and different designs will be evaluated at operating frequencies between 50 – 2000 Hz.

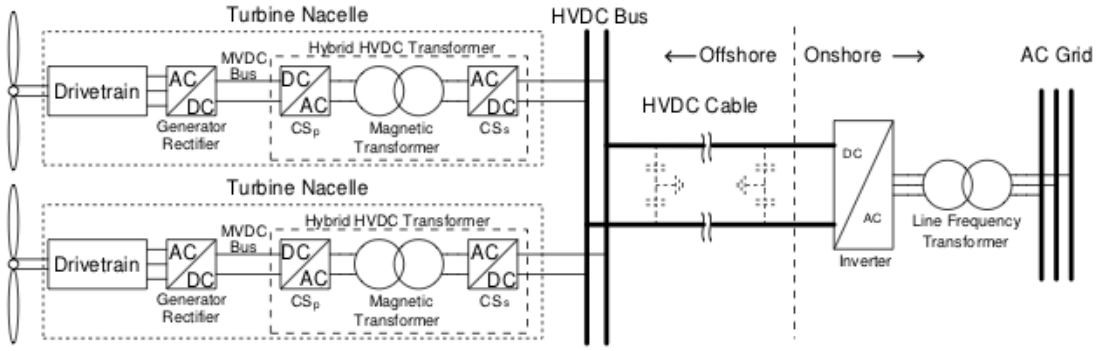


Fig. 3.1 Proposed wind turbine power train with Hybrid HVDC Transformer and potential HVDC grid layout with only 2 of the 5 proposed turbines shown

The inner MVDC bus voltage for turbines in use today is in the range of ±1 – 5 kV, depending on the manufacturer. The designed MVDC bus voltage is unlikely to change in the new generation of turbines, since much effort has gone into optimising the generator and variable speed converter. For the purposes of this study, the MVDC bus voltage for a 10 MW turbine is assumed to be ±5 kV, similar to the ABB PCS6000 MV wind turbine converter. The HVDC transmission voltage is assumed to be ± 320 kV, in line with several recent wind farm projects [156]. Considering the power level of each turbine, the switching losses would be unacceptable if the secondary bus voltage was 640 kV. It is therefore proposed that 5 turbines are series connected to form a mini cluster (Fig. 3.2) boosting the voltage up to the transmission level. In this way, the converter hardware can be better utilised, reducing both occupied space and losses.

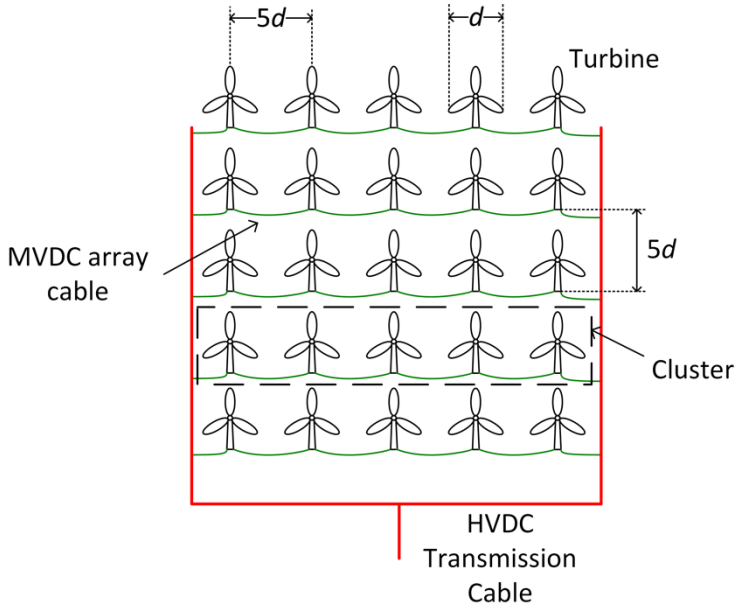


Fig. 3.2 Possible Hybrid HVDC Transformer wind farm topology using turbine clusters

The proposed mini-cluster topology is not without its own complications however. Controlling the power flow from each turbine and maintaining a stable DC grid may prove to be quite complicated and the redundancy of the overall system will be reduced. While this area is not discussed in detail in this thesis, it is proposed that this could form a follow up area of research in future. In any case, as previously discussed, it is likely that this Hybrid Transformer concept will first enter a MVDC market, as this simplifies some of the technical requirements of the transformer. As a result, each turbine would connected to the MVDC grid in parallel, simplifying the control and maximising redundancy.

3.2 Magnetic Loss Equation Comparison

As discussed in 2.2.3, non-linear core loss equations can be split into 3 groups, however, only empirical formula will be analysed in this section. Empirical formulae have been shown to be the simplest to implement using data provided by the manufacturers while still yielding accurate results. In industry, it is common practice to use the standard SE or use the SE with the FT of the flux waveform (FTSE). Since, despite their reported inaccuracies, they are simple to use. The predicted losses of these methods and the iGSE will therefore be compared to measured losses of a physical core under different operating conditions.

3.2.1 Core Loss Experiment Set-Up

There are many approaches to calculate core loss, each attempting to isolate the core losses from the winding and other parasitic losses. The set-up chosen to calculate the core losses for both characterisation and comparison purposes in this study is shown in Fig. 3.3

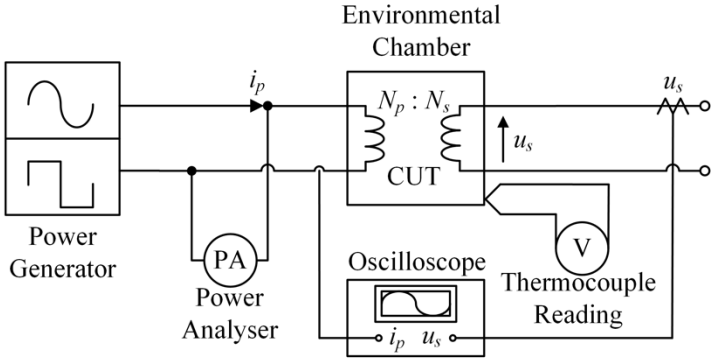


Fig. 3.3 Core loss experiment setup

A Pacific 360-AMX power generator was used to generate 5 test waveforms to investigate how accuracy changes with wave shape. The waveforms used, shown in Fig. 3.4 include: a

sine wave; distorted sine wave at 10% *THD*; a triangular wave and two square waves at 0.33 and 0.5 duty ratios (D = 0.33 and D = 0.5 square). Each waveform was repeated over a range of frequencies between 500 Hz and 2,000 Hz and voltages between 20 V and 60 V to test for sensitivity to both f_0 and $\hat{B}$. The generated waveform was verified by a Voltech PM6000 Universal Power Analyser and fed to the primary winding of the Core Under Test (CUT). Ferrite was chosen as the core material as this is a realistic material for this application, while still exhibiting enough losses to yield accurate results. The CUT was placed in a Weiss Technik SB Series environmental chamber set to 25 °C to maintain constant ambient conditions. A thermocouple, attached to the CUT logged its temperature to ensure the core temperature remained constant during testing.

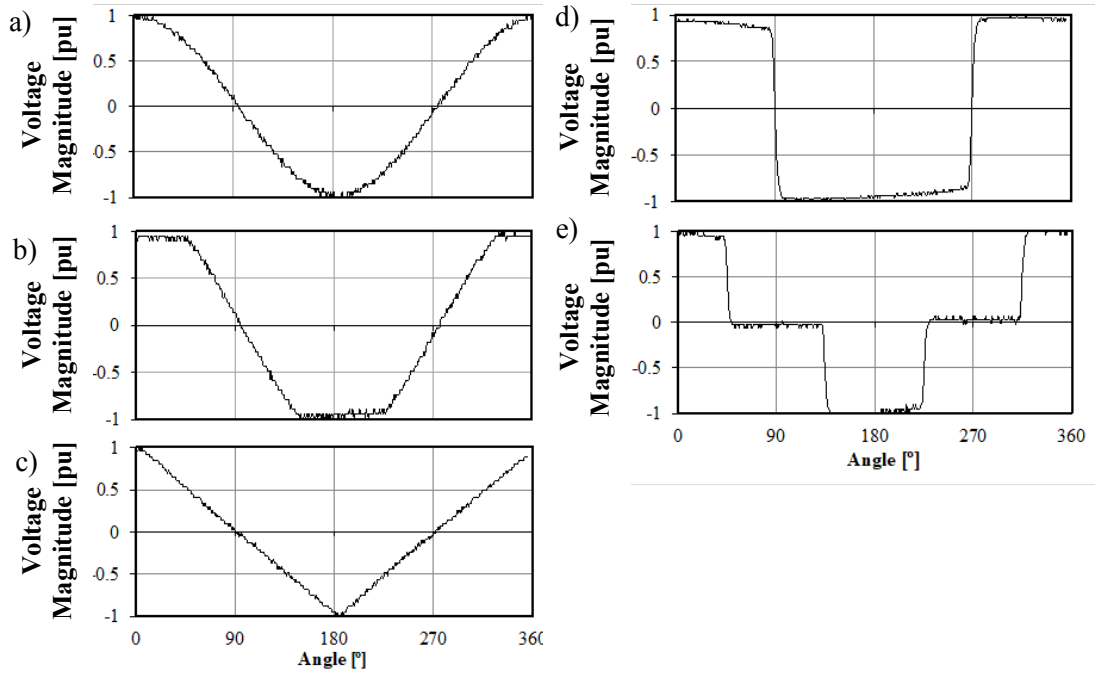


Fig. 3.4 Generated waveforms a) sine b) distorted sine c) triangular d) D = 0.5 square e) D = 0.33 square

The secondary winding of the transformer was open circuited. Four cycles of the primary current and secondary voltage were recorded using a Tektronix TDS 2024B oscilloscope. By measuring the open circuit secondary voltage, only the core losses were considered. The BH loop could then be directly calculated. This method is widely used in the literature due to its accuracy. From (2.55) and (2.59), Flux Density can be written as:

$$B = \frac{1}{N_s A_e} \int_0^{T_{cycle}} u(t)dt \tag{3.1}$$

and from (2.58), magnetic field strength can be expressed as:

$$H(t) = \frac{N_p i_p(t)}{L_e} \tag{3.2}$$

Which gives the core power loss per unit volume as (2.60).

The core manufacturer's datasheet only provides core loss information between frequencies of 25 kHz to 400 kHz. However, the frequencies of interest 500 Hz to 2000 Hz, lies far out with of this range. Therefore, the CUT needed to be characterised first to determine its Steinmetz Parameters over the range of interest. To accomplish this, sine waves between 500 Hz and 2000 Hz at flux densities of 0.05 T to 0.3 T were passed through the CUT. *H* was then calculated using (3.2) and the core loss from (2.60). These results were extrapolated to cover frequencies up to 4 kHz. The loss data from the datasheet covered the remaining 4 kHz to 10 kHz and 10 kHz to 25 kHz frequency ranges. The properties of the CUT are given in Table 3.1.

Manufacturer	Epcos
Material	N87 Ferrite
Shape	UI
L_e (m)	0.258
A_e (m^2)	8.4e^{-4}
N_p:N_s	92:37
V_c (m^3)	2.17e^{-4}
B_{sat} (T)	0.49

Table 3.1 CUT property table

A three-dimensional linear regression of the logarithm of (2.65) can then be used to calculate the Steinmetz Parameters for the frequency ranges shown in Table 3.2.

Frequency Range (Hz)	**Core 1**		
	k_{SE}	α	β
<1000	49.58	1.194	2.265
1000-4000	26.68	1.286	2.295
4000-10,000	267.2	0.774	1.472
10,000-25,000	1029	0.763	1.952
25,000-50,000	398.9	0.921	2.200
>50,000	71.31	1.114	2.338

Table 3.2 Calculated Steinmetz Parameters

With Steinmetz parameters computed, the core loss was calculated using the SE, FTSE and iGSE for each experiment variation. As several cycles were recorded for each variation, each cycle was separated for use with the SE and iGSE. The average core loss for each variation was taken to improve accuracy. The SE predicted core loss was then calculated from (3.3), after adaption from (2.65) for the i_l^{th} of n_c cycles in each experimental variation.

$$P_{core} = \frac{1}{n_c}\sum_{i_l=1}^{n_c} k_{SE} {f_0}_{i_l}^{\alpha} \hat{B}_{i_l}^{\beta} \tag{3.3}$$

To find the core loss through the FTSE, a Fast Fourier Transform (FFT) of $\hat{B}$ must first be performed to extract its harmonic components. The SE can then be applied to each component (1 to h_{max}) and summed using vector addition to determine the total core loss according to (3.4). As only four cycles could be recorded on the oscilloscope, the flux density vector was first extended ($\hat{B}ext$) to improve the FFT accuracy. This was achieved by repeating the recorded cycles, taking great care to stich the repeated cycles together properly so that the end of the last sequence led into the beginning of the next.

$$P_{core} = \sqrt{\sum_{h=1}^{h_{max}} \left(k_{SE_h} {f_0}_h^{\alpha_h} \hat{B}ext_h^{\beta_h}\right)^2} \tag{3.4}$$

By applying the algorithm described in Section 2.2.3, the flux density waveform was separated into its major and minor loops and the iGSE equations (2.66) – (2.67) applied. A weighted average (2.69) of each loop was used to calculate the total core loss over each cycle. The power loss was then averaged for the cycles analysed to improve accuracy as in (2.70). The results of all three methods were then compared to the experimentally obtained core losses to determine their respective accuracy.

3.2.2 Core Loss Experiment Results

The calculated core losses for the Epcos N87 core are presented here. The results are analysed for; constant input voltage, varying frequency and flux density; constant frequency, varying voltage and flux density; as well as constant flux density, varying voltage and frequency. The losses were calculated using experimentally obtained voltage and current measurements and three empirical methods; the standard SE, the FTSE and the iGSE. The measurements and calculations were repeated for five waveforms; a sine wave, distorted sine wave with a 10% *THD*, a triangular wave and two square waves, $D = 0.33$ square and $D = 0.5$ square.

It can be seen from Fig. 3.5 to Fig. 3.9 that all three empirical methods achieved the best results when used with a sinusoidal input voltage waveform. This is particularly true for the constant frequency case. As the *THD* of the input waveform increases towards 45% (the $D = 0.5$ square wave), the accuracy of the standard SE diminishes. This is to be expected as the SE is only valid for sinusoidal waveforms.

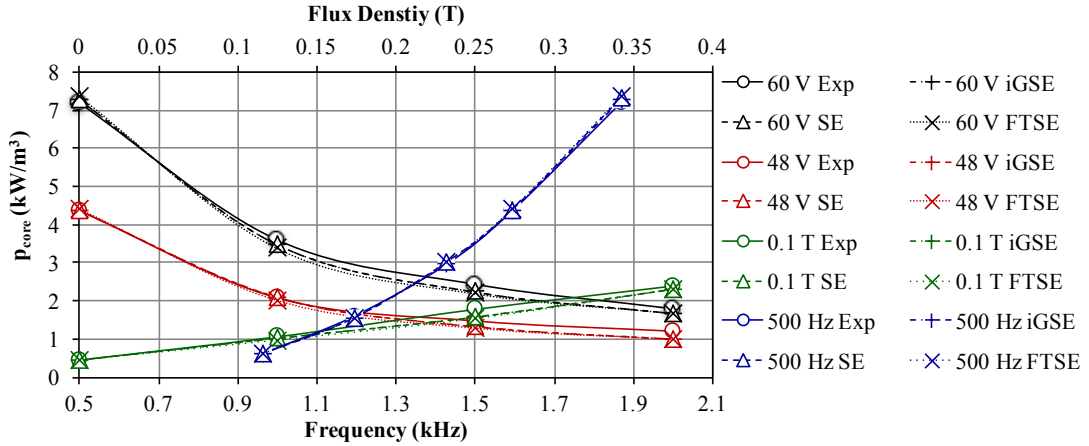


Fig. 3.5 Core losses for a sine wave determined from experimental results, the SE, FTSE and iGSE at different frequencies and flux densities

To compensate for the inaccuracy, many in the industry perform a Fourier Transform on the flux density waveform and use the SE on the result. This approach yielded relatively accurate results for the sinusoidal, distorted sinusoidal and triangular waves over all frequencies and flux densities but performed best at lower flux densities and frequencies.

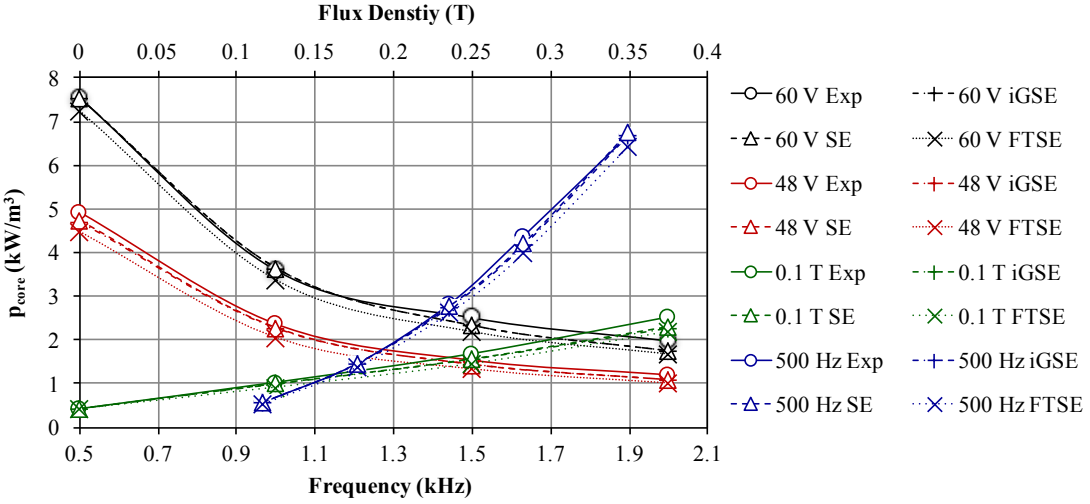


Fig. 3.6 Core losses for a distorted sine wave determined from experimental results, the SE, FTSE and iGSE at different frequencies and flux densities.

The iGSE performed well over all waveforms, frequencies, voltages and flux densities, matching the experimental data best in all but the D = 0.5 square wave. Here, somewhat surprisingly the standard SE performed marginally better. Both the SE and FTSE performed best between 500 Hz and 1000 Hz achieving errors of around ±5% for the sinusoid, distorted and triangular waveforms. The iGSE continued to perform well for the D = 0.33 square wave

with errors <±5% but this increased for the $D = 0.5$ case to around ±7%. The SE had errors of ±5% for the $D = 0.5$ square wave however, this increased to ±8% for the $D = 0.33$ square wave.

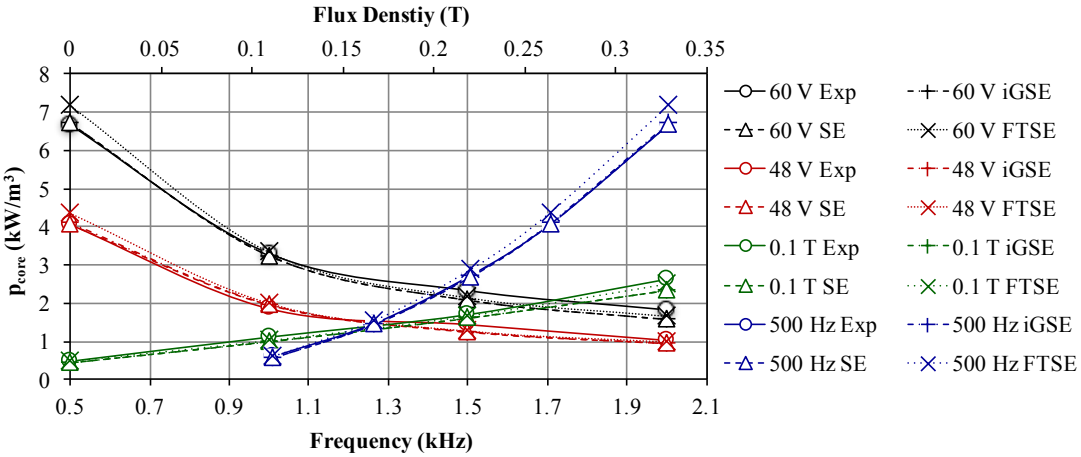


Fig. 3.7 Core losses for a triangular wave determined from experimental results, the SE, FTSE and iGSE at different frequencies and flux densities

The error for all methods increased for frequencies above 1000 Hz, in some cases by a factor of 2. However, this is likely due to a poorer fit of the calculated Steinmetz parameters as discussed later. This highlights the importance of obtaining accurate Steinmetz parameters. A safety factor (S_f) of around 5% should be used if there is a high degree of confidence in the values of the Steinmetz parameters. Otherwise, a S_f of 10% should be used with the SE and iGSE methods. While the error of the FTSE is similar to that of the SE and iGSE for the sinusoid and triangular waves, it increases to around ±45% in the square wave cases.

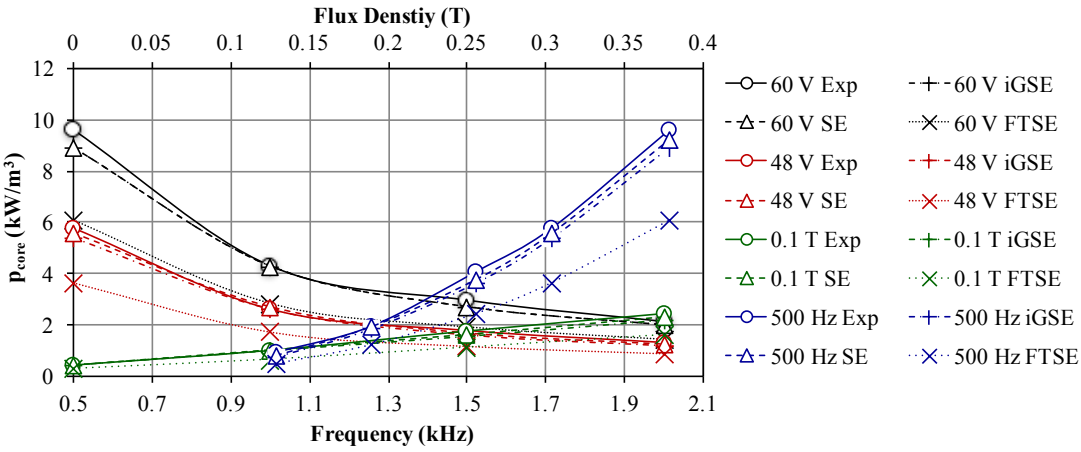


Fig. 3.8 Core losses for a 0.5D square wave determined from experimental results, the SE, FTSE and iGSE at different frequencies and flux densities

In both constant voltage sets (60 V and 48 V) the power loss decreases with increasing frequency. This is due to the peak flux density decreasing with frequency (3.1). It can be seen

from Table 3.2 that the flux density exponent (β) is greater than that of frequency (α) resulting in an inverse relationship with frequency. If either flux density or frequency is held constant, the power loss increases with increasing frequency and input voltage respectively.

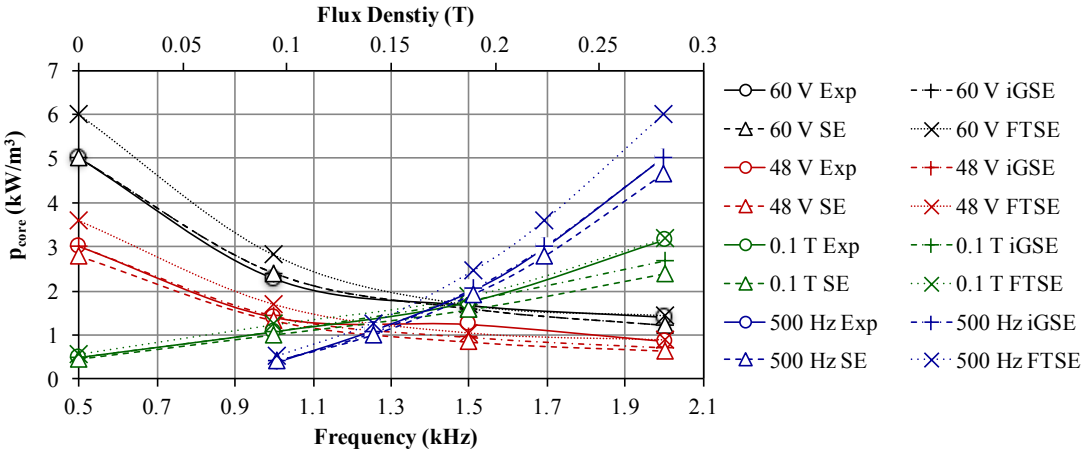


Fig. 3.9 Core losses for a 0.33D square wave determined from experimental results, the SE, FTSE and iGSE at different frequencies and flux densities

3.2.3 Core Loss Equation Discussion

As can be seen from Fig. 3.10, the Steinmetz parameters obtained for frequencies below 1 kHz offered a closer fit to the measured core losses for all flux densities. The consequence of this can be seen in the experiment results presented in Fig. 3.5 to Fig. 3.9 but is particularly evident for the sinusoidal case shown in Fig. 3.5. Here it can be seen that at the lower frequency end of the constant voltage and constant flux density waveforms, the error in the empirical calculations is smaller. Better results were also achieved from the constant frequency sets as they were taken at 500 Hz.

It can also be seen in Fig. 3.10 that the core behaves oddly around 1.5 kHz. This point was retested and the results proved repeatable. Additional measurements were taken around 1.5 kHz to better characterise the behaviour. The calculated power loss from the additional measurements showed that the core loss also reduced from that predicted by the SE immediately around the 1.5 kHz data point. The cause of this deviation from the predicted power loss at 1.5 kHz is unclear but it occurs for all flux densities and proved repeatable so is unlikely to be a result of measurement error. The consequence of this is a reduced accuracy of the loss predicted by the Steinmetz Equation in Fig. 3.10 around this frequency and the general reduction in accuracy above 1000 Hz observed in Fig. 3.5 to Fig. 3.9.

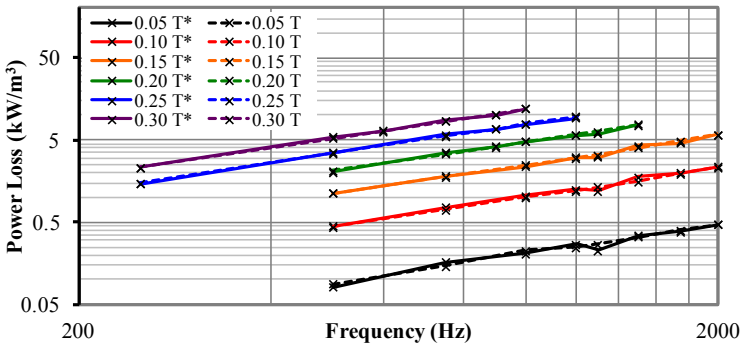


Fig. 3.10 Measured and Steinmetz Parameter predicted core losses from 250 Hz to 2000 Hz and 0.05 T to 0.3 T. Experimentally measured results have a * suffix in the figure key

While the error of the SE and FTSE in the triangular wave case was surprisingly low, it can be explained as follows. The SE is based on the flux density waveform and not that of the voltage waveform; from (3.1) the flux density is obtained from the integral of voltage. The resulting waveform therefore has a relatively low *THD*. Waveforms with a low *THD* are often used with the standard SE resulting in a relatively accurate representation of core losses for both the 10% *THD* and triangular waveforms.

As evident in Fig. 3.8. & Fig. 3.9 the FTSE becomes highly inaccurate, less so even than the standard SE. While the literature suggests that it would be inaccurate due to the non-linearity of the SE, the extent of the error was still surprising. Further investigation revealed that, while the FFT picked out the correct frequencies of each harmonic, the magnitude of the components differed significantly from the original waveform in the square wave cases. As the flux density is raised to a power between 1.4 and 2.3 (Table 3.2) in the SE this error is magnified, significantly affecting the results. It is known that the component magnitudes are often less accurate than their frequencies and many windowing techniques exist to improve its accuracy. It is possible therefore that better results may be obtained through applying an appropriate window to the results. Increasing the resolution of the measurement data may also improve the results, although voltage and current readings were already taken at the relatively high frequency of 0.25 MHz to 1 MHz

It is thought that the source of this inaccuracy is the requirement of an infinite number of harmonic components to accurately represent the energy contained in each component of highly non-linear flux density waveforms generated by square waves. Since it is not possible to create an infinite number of harmonics, the energy is incorrectly distributed across them, leading to an error in the magnitude of the attributed flux densities.

It might be expected that the accuracy of the iGSE for the D = 0.33 case would decrease compared to that of the D = 0.5 case due to relaxation effects. From Fig. 3.8 – Fig. 3.9 however, this does not appear to be true as the error increases for the D = 0.5 case. This may be because the increase in error caused by the effect of magnetic relaxation is small compared to that caused by the increase in *THD* in this example. However, the balance may well shift if the number of rapid changes in the core's magnetization is increased, such as would be experienced due to pulse width modulation.

3.3 Magnetic Transformer Design

With the core loss calculation method determined, a computer model of the Hybrid Transformer can be developed for different designs and operating conditions. This section concerns the design of the magnetic transformer and windings, first describing the parameters that are kept constant for each design criteria, such as core shape and winding type. The optimisation process used to determine the transformer design for increasing frequencies and number of primary turns is then detailed.

3.3.1 Core Choice and Winding Design

The optimum core shape for the Hybrid HVDC Transformer was selected based on Table 2.5. Due to high currents in the primary winding, a 3-phase design has been chosen. Toroidal and Matrix cores are ruled out as viable options due to cooling difficulties and large core volume respectively leaving U and E-core designs. From Section 2.2.2, the 3-phase design transformer cores require less material than 3 single-phase transformers. For example, three U-cores have 2 additional legs when compared to a single, 3-phase E-core. Therefore, the E-core was chosen to minimise the core volume and cost while maximising power density and efficiency.

The winding choice and construction influences both the transformer losses and volume. From (2.72) the skin depth in the MF range is calculated to between 1.45 and 2.9 mm assuming a current density of 4 A/mm^2. If the modulation index of the converter is M = 0.9 then the RMS primary and secondary currents are $i_{p_{rms}} = 1053\ A$ and $i_{s_{rms}} = 16.5\ A$ which gives the minimum primary and secondary winding radii as $r_p = 263.2$ mm and $r_s = 4.1$ mm. Therefore, R_{ac} will have a significant effect on the primary winding losses and so only stranded and foil type windings can be considered. While stranded windings and especially litz wires have very low losses, they are also very expensive and have the lowest packing factor, increasing the volume of the transformer (Table 2.6). This will be exacerbated by the high

current on the primary, requiring many strands to achieve an acceptable current density. Foil windings have a very high packing factor however, and an acceptable R_{ac} and so have been selected for the primary winding. As the secondary current is so small, it is unaffected by R_{ac} and so standard AC cabling can be used.

3.3.2 Transformer Dimensions

The optimum dimensions of the transformer are heavily dependent on the operating frequency. Therefore, to fairly compare the performance of the transformer over the MF range, the magnetic transformer dimensions must be allowed to change. This was done through use of an algorithm (Fig. 3.11) which used the transformer voltage and current waveforms generated by the Simulink model as well as the transformer inputs to determine its parameters.

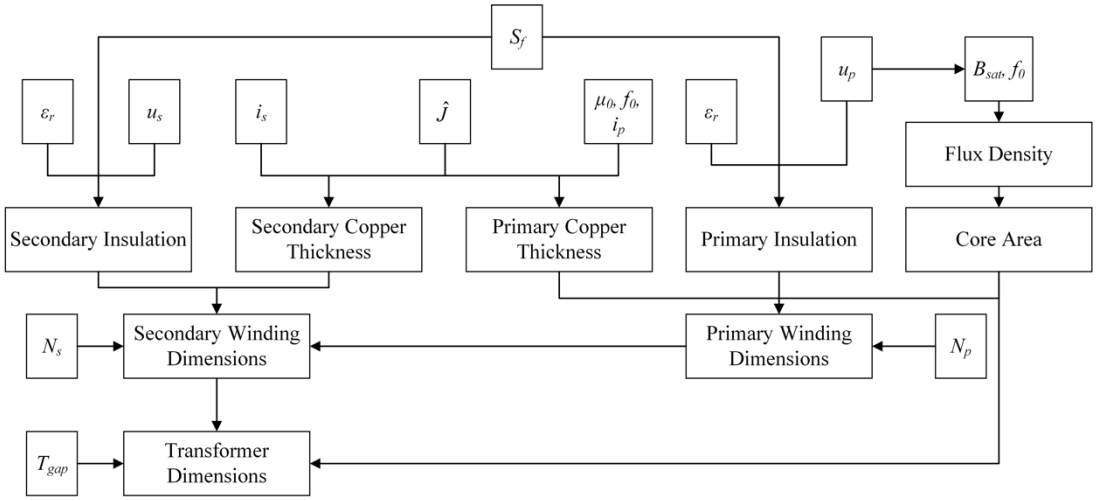


Fig. 3.11 Flow diagram of transformer design algorithm

First, the maximum flux in the core is calculated from (2.55); assuming that the maximum permitted flux density is 90% of the saturation flux, A_e is given by:

$$A_e = \frac{|\hat{\theta}|}{\hat{B}} \tag{3.5}$$

From Fig. 3.12 the outer primary radius and winding length (r_p and l_p) can be calculated from (3.7) and (3.8) for a given dielectric field strength (ϵ_r).

$$r_p = T_{bob} + T_{in} + T_{ps} + N_p(T_p + T_{pi}) - T_{pi} \tag{3.6}$$

$$r_p = \frac{\sqrt{Ae}}{\sqrt{2}} + \frac{U_{dc}^p}{2\epsilon_r} S_f + \frac{U_{dc}^s + U_{dc}^p}{2\epsilon_r} S_f + N_p\left(d_{cp} + \frac{U_{dc}^p}{N_p \epsilon_r} S_f\right) - \frac{U_{dc}^p}{N_p \epsilon_r} S_f \tag{3.7}$$

$$l_p = 2\pi N_p \left(R_{in} + \frac{N_p}{2}(T_p + T_{pi}) \right) \tag{3.8}$$

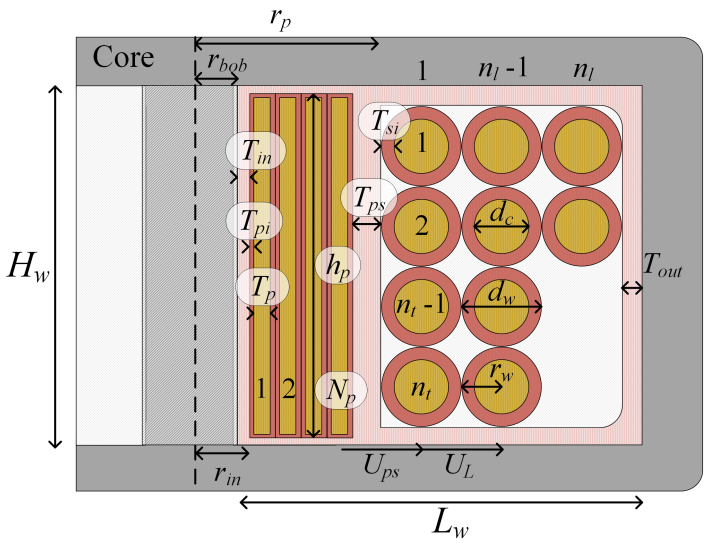


Fig. 3.12 Transformer winding configurations for one phase of the Hybrid Transformer

The height of the core window is determined by the height of the primary winding given by:

$$h_p = h_s = \frac{\hat{\imath}_p}{\hat{J}\,T_p} + 2T_{pi} \tag{3.9}$$

Where $\hat{J}$ is the maximum current density allowed and $\hat{\imath}_p$ is the peak winding current. From Fig. 3.12 the number of secondary turns per layer can be calculated and hence the required secondary wind insulation thickness (T_{si}).

$$h_s = n_l d_w \tag{3.10}$$

$$h_s = S_f \frac{2U_{dc}^s}{N_s \epsilon_r} n_t^2 + \sqrt{\frac{4\hat{\imath}_p}{\pi \hat{J}}} n_t + 2T_{out} \tag{3.11}$$

$$n_t = \left\lfloor \frac{-\sqrt{\frac{4\hat{\imath}_p}{\pi \hat{J}}} + \sqrt{\frac{4\hat{\imath}_p}{\pi \hat{J}} + 4\left(S_f \frac{2U_{dc}^s}{N_s \epsilon_r} . \left(h_{s_{min}} - 2T_{out} \right) \right)}}{2S_f \frac{2U_{dc}^s}{N_s \epsilon_r}} \right\rfloor \tag{3.12}$$

$$n_l = \frac{N_s}{n_t} \tag{3.13}$$

$$T_{si} = \frac{U_{dc}^s}{n_l \epsilon} S_f \tag{3.14}$$

The mean secondary winding length is more complicated to calculate than the primary as there are not necessarily an integer number of layers, therefore it is given by:

$$l_s = 2\pi n_t \lfloor n_l \rfloor \left(r_p + \lfloor n_l \rfloor r_s\right) + 2\pi n_t (\lceil n_l \rceil - n_l)\left(r_p + T_{gap} + (2\lceil n_l \rceil - 1) r_s\right) \tag{3.15}$$

Where $\lfloor x \rfloor$ denotes the floor of x and $\lceil x \rceil$ the ceiling. The outer radius of the windings (r_s) is simply:

$$r_s = r_p + 2n_l r_s + T_{out} \tag{3.16}$$

The core window length and height from Fig. 3.13 are therefore

$$L_w = 2\left(\left(r_s - \frac{\sqrt{A_e}}{2\sqrt{2}}\right) + T_{gap}\right) \quad H_w = h_p \tag{3.17}$$

and hence the core (V_{core}) and magnetic transformer volume (V_T) are then:

$$V_{core} = \left(2L_w + 3\frac{\sqrt{A_e}}{\sqrt{2}}\right) \cdot \left(H_w + \sqrt{2}\sqrt{A_e}\right) \cdot \frac{\sqrt{A_e}}{\sqrt{2}} \tag{3.18}$$

$$V_T = \left(6r_s + 2T_{gap}\right) \cdot \left(H_w + \sqrt{2}\sqrt{A_e}\right) \cdot 2r_s \tag{3.19}$$

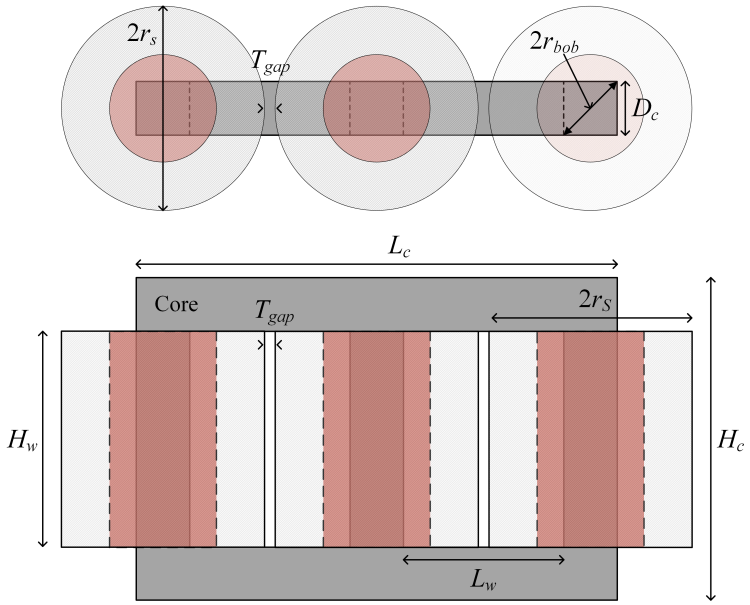


Fig. 3.13 Overall dimensions of the 3-phase Hybrid Transformer from aerial and front on perspectives

3.3.3 Transformer Loss

With the transformer parameters now known for each frequency and number of primary turns, the core and winding losses can be calculated. In accordance with Section 3.2.1, the iGSE was used for the core loss calculation, applying the Steinmetz parameters presented in Table 3.3.

Frequency (Hz)	k	α	β
<1000	49.58	1.194	2.265
1000-2000	26.68	1.286	2.295

Table 3.3 Calculated Steinmetz Parameters for N87 Ferrite Core

The specific core loss was then calculated from (2.66) – (2.70)where the time varying flux density in the transformer core derived from the transformer voltage waveform using (3.1). The total core loss is then simply:

$$P_{core} = V_{core} \cdot P_{iGSE} \tag{3.20}$$

To calculate the winding losses, the primary and secondary winding resistances (R_p and R_s) must first be calculated. The AC resistance of the primary winding is given by (2.74) – (2.75) and the DC resistance of the secondary by (2.71). As the current may not be completely sinusoidal, the true Root Mean Square (RMS) value of the current should be used to calculate the power losses of the primary and secondary as in (3.21) – (3.22).

$$P_p = R_p \sqrt{\frac{1}{T_{cycle}} \int (i_p)^2 dt} \tag{3.21}$$

$$P_s = R_s \sqrt{\frac{1}{T_{cycle}} \int (i_s)^2 dt} \tag{3.22}$$

3.4 Converter Comparison

In this section, the efficiencies, harmonics and stability of various converter topology combinations are analysed to determine the optimal configuration for the Hybrid HVDC Transformer. After an initial analysis of the available converters, detailed MATLAB/Simulink models are used to compare the shortlisted topologies over a range of frequencies and power levels.

3.4.1 Initial Converter Selection

To simplify the analysis and due to the high current on the primary side, only 3-phase configurations of the converter topologies shown in Table 2.1, are considered. A decision

matrix is used to narrow down the remaining topologies (Table 3.4). There are four key requirements the Hybrid HVDC transformer:

- Efficiency
- Volume
- Control Stability
- Reliability

which are explained in more detail below.

If the Hybrid HVDC transformer is to be considered a viable alternative it must be at least comparable to the conventional solution. Due to the high-power density of the converter and tight space requirements, it is also desirable to minimise the heat generated by the converter. The converter topology not only determines the switch count but also the required switching frequency, filter requirement and *THD* of the flux waveform and hence also influences magnetic losses.

As mentioned, the Hybrid Transformer must fit within a confined space and so volume is important. This is not only influenced by the number of switches in the converter but also by ancillary components e.g. additional transformers, filters or capacitors. Furthermore, converters with a high degree of modularity are known to be more compact and easier to construct.

To maintain control stability of the turbine it is important to accurately manage the power flow through the device. For sinusoidal waveforms, this is controlled through selection of X' for u_p and u_s' voltage as in (3.23). The angle between u_p and u_s', δ, then determines the power transferred (P_T).

$$P_T = \frac{u_p u_s' sin\,(\delta)}{X'} \tag{3.23}$$

The converter choice and filter size will determine the quality of the AC waveform and hence also the stability of the control as any injected harmonics will influence P_T.

Reliability of offshore equipment is imperative due to the expense and time between maintenance operations. Failure rates are often highest soon after installation due to faults in the construction and control. Simpler designs are therefore preferred to minimise these failures. After the settling-in period, the failure rate falls but will be influenced by components failing before their design life. In power electronics, this is heavily influenced by over-current and voltage transients. Due to inherent inductances and capacitances within gate drives and switches, there is a delay between the generation and execution of a gate signal. Each

component therefore has a specified response time and tolerance. This causes problems when many switches are connected in series to support a high voltage stress, as each one must turn on or off simultaneously to prevent a temporary uneven distribution of voltage stress through the valve. Since this is not possible due to the tolerance on the response time of each switch, some switches will be subjected to a higher stress during each switching cycle. This can be mitigated through careful selection or custom designed components to reduce the tolerance, by increasing the number of devices in the valve or by increasing the switch rating. However, each option increases the cost of the converter though and does not eliminate the issue. There is therefore a practical limit to the number of switches that can be connected in series.

It can therefore be seen that adherence to the four key requirements described above can be measured based on the parameters shown in Table 3.4. In this table, conduction loss is based on the number of components conducting at any one time, switching loss is determined by the switching frequency to achieve a given filter size, converter components refers to the number of switches, diodes and capacitors required with capacitors weighted more heavily and ancillary elements refers to DC sources (transformers) and AC/DC filter requirements.

Category	**Converter Topology**				
	FB	NPC	FCC	CHB	MMC
Conduction Loss	5	3	4	2	1
Switching Loss	1	3	3	3	5
Converter Components	5	2	2	4	1
Ancillary Elements	3	4	4	1	5
THD	1	3	3	3	5
Nº Series Switches	1	3	3	3	5
Circuit Complexity	5	1	2	3	5
Control Complexity	5	4	3	4	1
Total	**26**	**23**	**24**	**23**	**28**

Table 3.4 Decision matrix of common converter topologies

The converters were given a score of 1 to 5 for each category with 5 being the best. After summing up each converter's score, the FB and MMC can be seen to have the highest score. This provides a very crude method of comparison however, as not all categories will necessarily have an equal impact and the ratings are qualitative. A quantitative comparison will result in a much better comparison but requires a time consuming, detailed analysis of each topology. This would have taken too long so a first pass qualitative approach was taken to narrow down the potential topologies to two, before performing a quantitative analysis. From Table 3.4, not only are the FB and MMC ranked highest, their scores in individual categories suggest that they could provide an interesting comparison. For example, the MMC ranks very highly in switching loss and THD, while the FB does well in conduction losses and converter components. For these reasons, the MMC and FB were selected for further analysis.

3.4.2 Switch Selection

The switch choice has a significant effect on the overall performance and cost of the converters and so was considered carefully. To this end, the component library has been minimised through use of the same switch on the primary and secondary converter to reduce construction and maintenance costs. To provide black start capabilities and allow full control, only gate commutated switches were considered. While the Integrated Gate Commuted Thyristor (IGCT) has low conduction losses its switching losses prohibit it from operating in the medium frequency range. Power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) can operate at very high frequencies; however, their power ratings are still too low (≈ 200 W). Integrated Gate Bipolar Transistors were therefore selected as they have reasonable conduction and switching losses in the MF range.

Considering the FB and MMC topologies there are four potential configurations for the Hybrid HVDC Transformer. The FB or MMC can be used on both the MV and HV sides (FB-FB, Fig. 3.15a and MMC-MMC, Fig. 3.15b respectively) or a novel, hybrid configuration with the FB or MMC on the MV and the other topology on the HV side could be used. With the practical difficulties of connecting many IGBTs in series, the FB-MMC configuration (Fig. 3.15c) may hold significant advantages over both the FB-FB and MMC-MMC topologies. On the MV side the simplicity and low component count of the FB can be utilised, while on the HV side the modularity, reduced series connection of switches and low *THD* of the MMC may prove beneficial. This therefore plays to the strengths of both topologies while there are no perceived advantages for the MMC-FB configuration. The performance of the FB-MMC will therefore be tested against the FB-FB and MMC-MMC.

3.4.3 Converter Model Parameters

Computer models were developed for the FB-FB, MMC-MMC and FB-MMC configurations in the MATLAB/Simulink environment and are shown in Fig. 3.14 and Fig. 3.15. It is assumed that the MVDC bus voltage is designed to vary by ± 10% to provide reactive power support. A safety factor of 50-60% has also been used for both the MV and HV converters to allow for transients and provide redundancy in case of switch failure and for cosmic radiation failure [157]. Therefore, the number of modules required on the primary can be calculated as 4 with 50 on the seconday.

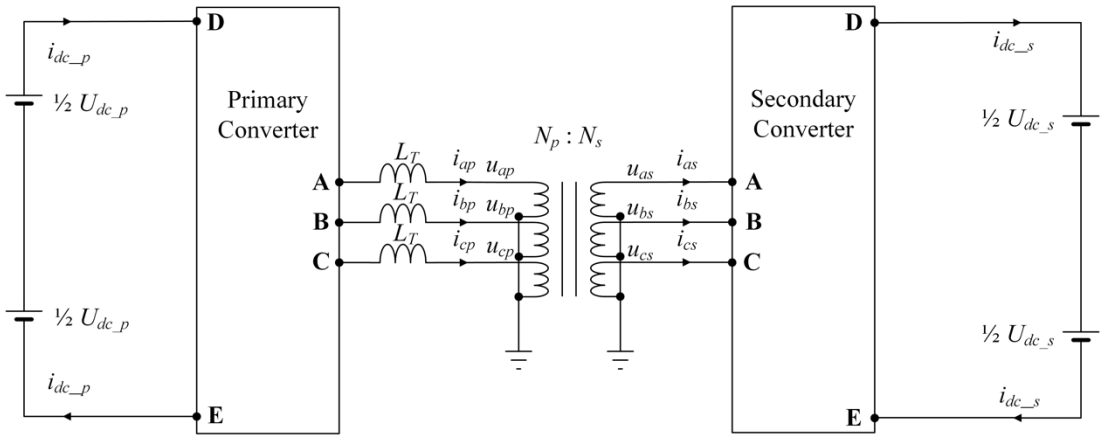
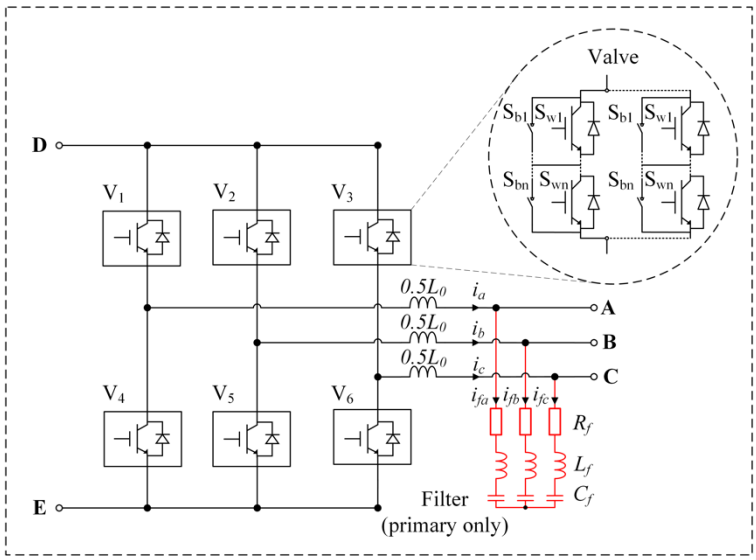
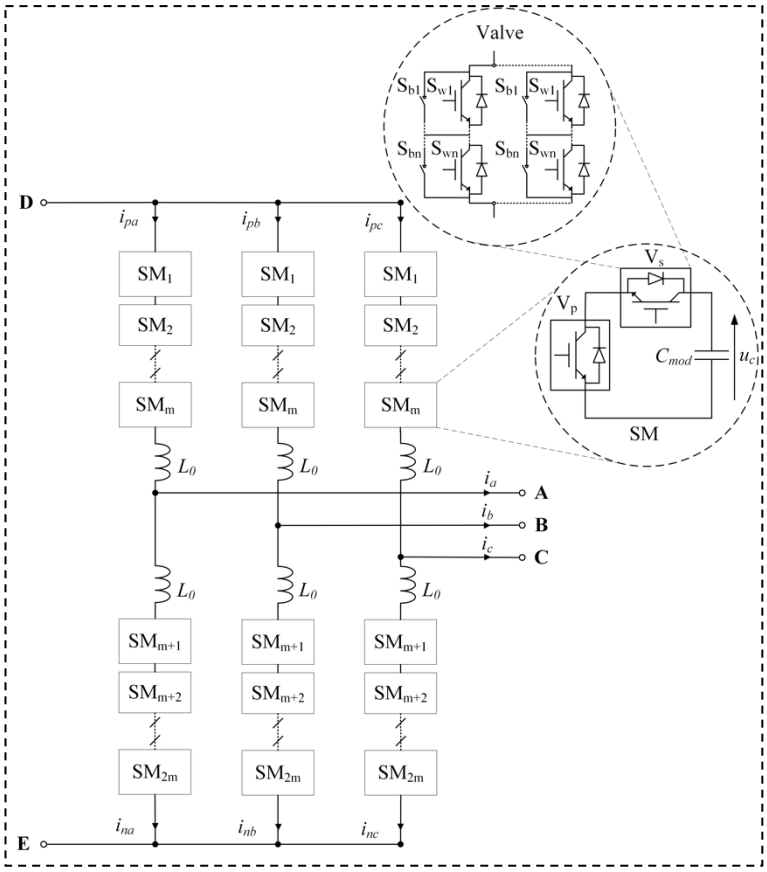


Fig. 3.14 The generic MATLAB/Simulink model used to evaluate each of the transformer configurations



a)



b)

Fig. 3.15 The converter models used in each of the transformer topologies including the a) FB converter and b) MMC

Ideal IGBT/diodes are used throughout the model, as the non-linear relationship between resistance, switching loss and current in semiconductors cannot be accurately accounted for in the simulation. The ideal IGBT/diode does not consider the forward voltages or the physical dimensions and complex behaviour of the devices. Instead, empirical formulae were defined from the manufacturer's datasheets, relating the arm current to switching loss and the voltage potential across the IGBT.

These empirical formulae were then used to calculate the switching and conduction losses based on the arm current at each relevant time step.

Due to the high level of harmonic distortion injected by the FB converters, PWM is used in conjunction with two double tuned notch filters and a high pass filter to allow full control of real and reactive power flow through the transformer. Notch filters were chosen for the lower end harmonics as their resonant behaviour minimises both losses and volume. Due to the operating frequency, a relatively low PWM ratio of 21 was used to lower the switching losses.

As a result, a high quality factor (q_f) of 150 is required in the notch filters to have a significant effect with the high pass filter at a lower value of 5 to ensure a broad filter range. The first double band filter is tuned to $f_{cr} \pm 2f_0$ with the second at $2f_{cr} \pm f_0$ to cover the peak side bands, the high pass filter is tuned to $3f_{cr} - 3f_0$. The reactive power injection of each filter is 7 %, 4% and 0.9% of the rated transformer power respectively.

With each switch having a rated collector emitter voltage (V_{ce}) of 4.5 kV and each turbine supporting a DC bus of 128 kV, 50 SMs are in the secondary MMC. The large computation time required to run a high fidelity 40 SM MMC is impractical and so an averaged model was used to simulate the MMCs. An explicit controlled voltage source based model was selected for this purpose from the model types covered in Section 2.1.3.3 since:

- It solves considerably faster than high fidelity models especially when many SMs are present
- It has been shown to be good for investigating control algorithms
- It can handle additional complexities at the AC terminals such as star connected transformers

As the converter is operating in the MF range, the voltage ripple can be reduced by increasing the SM capacitance without significantly affecting the converter size. The C_{mod} for the MMCs are therefore calculated using (2.52) to generate a 5% capacitor voltage ripple at each operating frequency. The resonant arm inductance was then calculated from (2.53) and L_0 selected to be 3 times greater to avoid any resonant interaction with the SM capacitors. The converter specifications are summarised in Table 3.5 with their circuit diagrams shown in Fig. 3.15.

Converter Type	FB	MMC
N_{vp}	4	1
N_{vs}	40	1
Allowable capacitor voltage ripple (MMC)	N/A	5 %
L_0 **ratio (MMC)**	N/A	3
P_{ref}	10 MW	
f_0	0.05 – 2 kHz	
U_{DCp}	10 kV	
Transmission voltage	640 kV	
Nº turbines in cluster	5	
U_{DCs}	128 kV	
IGBT	ABB 5SNA 0650J450300	
V_{CE}	4.5 kV	
I_{CE}	600 A	
a	1:14	
Samples/cycle	500	

Table 3.5 Summary of the converter specifications used for the comparison

3.4.4 Converter Control

Standard dq0 control algorithms are used to control the power and current flow through the converters based on the measured AC voltage and current on the primary side. In all configurations, the primary converter is used to control power flow, while the secondary converter is passive. In addition to power control, the MMC has a CCS and a reduced switching frequency PSC-PWM voltage balancing algorithm as described in Section 2.1.2 – Section 2.1.3.

The current and power controller shown in Fig. 3.16 was developed from (2.29), (2.30) and (2.33), (2.34) to be used in the analysis. Similarly, the CCS control was created from (2.36), (2.37) and is shown in Fig. 3.17.

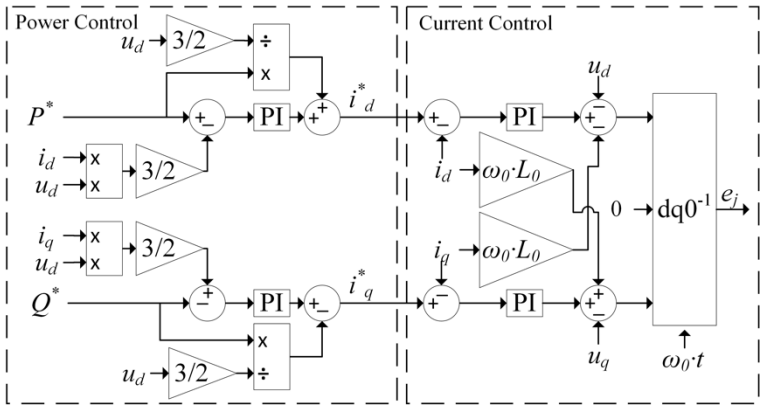


Fig. 3.16 Outer power and inner current dq0 control used by the MMC and FB converters

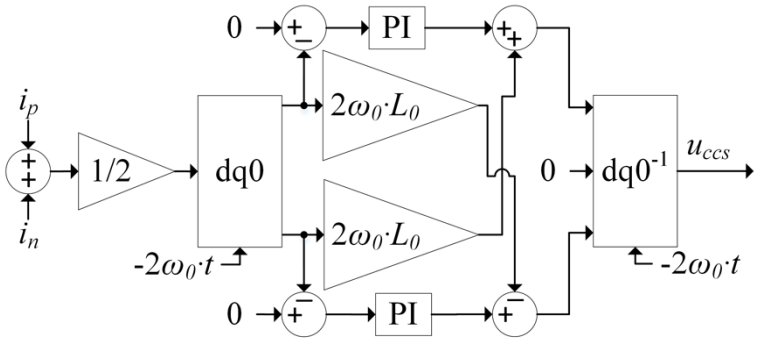


Fig. 3.17 Circulating Current Suppression dq0 control used by the MMC

3.4.5 Converter Loss Calculation

The results from the model simulations were exported to MATLAB where the average steady state conduction, switching and core losses were calculated. The IGBT junction temperatures were assumed to be 125°C throughout the steady state operation. In reality, the operating

temperature may vary but it would remain close to the maximum operating temperature if the system operates close to the rated power.

As mentioned the switching and reverse recovery losses (P_{sw}, P_{rr}) as well as V_{ce} in semiconductors vary non-linearly with the collector current (i_c). The manufacturer's datasheets were therefore used to determine each of the N_{sw} IGBT's collector emitter and forward diode voltages (u_{ce} and u_f). The P_{sw} and P_{rr} with respect to i_c at each of the n_{st} time steps and hence determine the conduction and switching losses of each valve (P_{conv} and P_{swv}) can then be calculated from:

$$P_{con_v} = f_0 \sum_{i_t=1}^{n_{st}} i_{c_t} \left(u_{ce_{i_t}} + u_{f_{i_t}} \right) N_{sw} T_{step} \tag{3.24}$$

$$P_{sw_v} = f_0 \sum_{t=1}^{T} \left(P_{sw_t} + P_{rr_t} \right) N_{sw} T_{step} \tag{3.25}$$

The total converter losses, P_{tot} can then be calculated from the sum of losses for each valve number, v where n_v is the total number of valves in the converter:

$$P_{tot} = \sum_{v=1}^{n_v} P_{con_v} + P_{sw_v} \tag{3.26}$$

The inefficiencies generated by the notch filter in the FB converters can be calculated from the power difference between the filter inductor and the transformer at the fundamental frequency.

3.5 Transformer Comparison Results and discussion

The total losses for each transformer configuration are plotted in Fig. 3.18 – Fig. 3.20 against frequency and shows that as expected, the losses increase significantly with frequency for each converter especially in the FB-FB case. In all three cases above 100 Hz, the switching losses of the primary converter contribute the most to the overall losses. This is particularly true for the MMC-MMC and FB-MMC cases (Fig. 3.17 and Fig. 3.18) where only the primary converter is operated using PWM. Indeed, at 100 Hz, the primary switching losses in the FB-MMC configuration account for over 50% of the total losses, increasing to over 90% by 2000 Hz. In the FB-FB case (Fig. 3.19) both converters are operated using PWM; and the secondary converter losses are slightly larger.

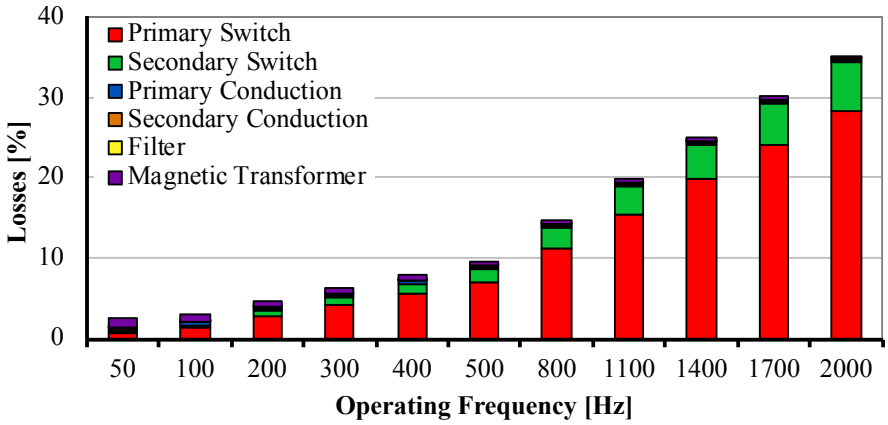


Fig. 3.18 Total transformer loss for the MMC-MMC with 5 turns on the primary

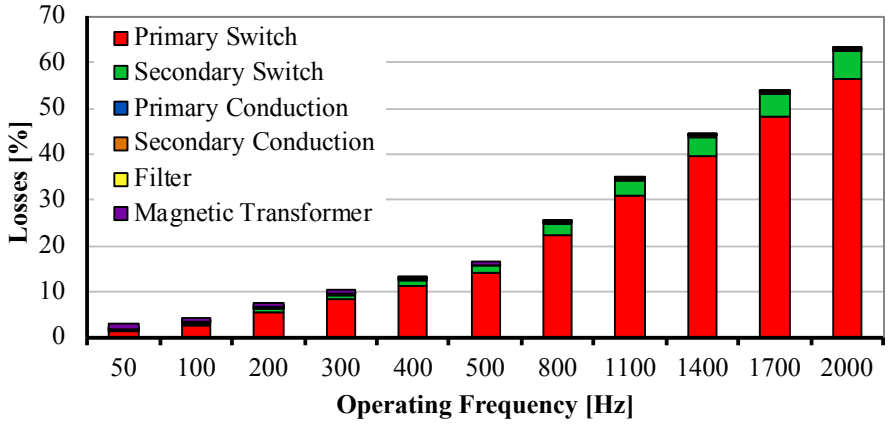


Fig. 3.19 Total transformer loss for the FB-MMC with 5 turns on the primary

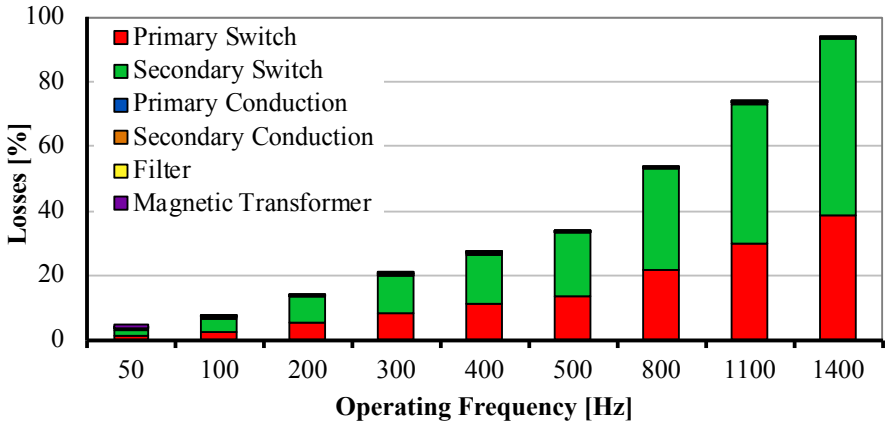


Fig. 3.20 Total transformer loss for the FB-FB converters with 5 turns on the primary

An argument could also be made to use soft switching. Soft switched converters are hard to design in practice however, and are normally tuned for a specific operating condition. In a wind turbine, where the power output varies significantly from its cut-in wind speed up to its rated wind speed and DC bus voltage can vary by 10%, reduced switching losses would be rarely realised. Furthermore, outside the converter's design region, the additional losses caused

by the resonant banks could increase the converter conduction losses not to mention increase the converter size. As a result, soft switching was not considered in this analysis and so to operate within the medium frequency range, the converters should operate using NLM. To do this; however, more voltage levels must be created by the primary converter which could be difficult due to the restricted DC voltage range.

A contributing factor to the lower losses of the MMC topology compared to the FB can be seen in Fig. 3.21. From (2.15) & (2.16), it is known that the MMC's arm current contributes to half of the output current with any discrepancy due to the DC component (as the second order harmonics have been cancelled). In the FB case however, the peak current through each arm is equal to the peak output current with the addition of harmonic currents. The current waveforms generated by the FB and MMC are shown for comparison. As a result, the FB switches are subjected to higher currents and hence higher losses per switching operation.

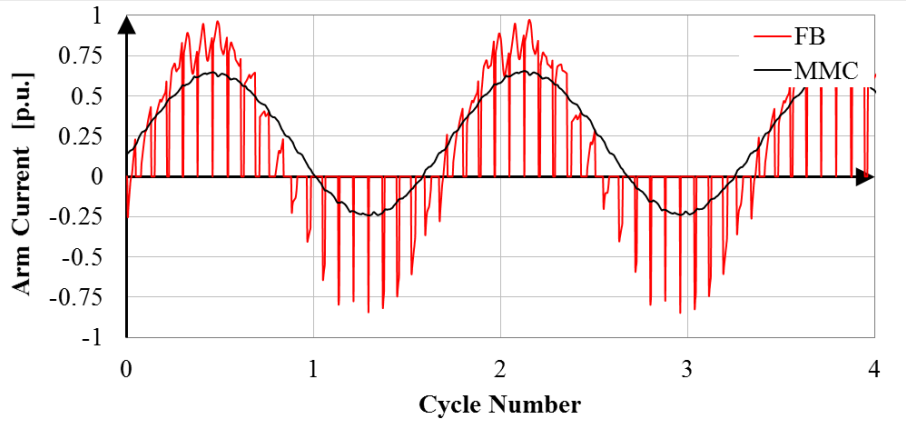


Fig. 3.21 Arm current waveforms for the FB and MMC at 500 Hz

That said, with half the number of switches and no SM capacitor, the converter is more compact than the MMC (Fig. 3.22). At 50 Hz, the primary MMC is 2.4 times the size of the FB, this reduces to a factor of 2.1 at 2000 Hz since the SM capacitance of the MMC reduces. At low operating frequencies, the magnetic transformer makes up more than 95% of the total volume but reduces to less than 50% at 2000 Hz. Therefore, the larger magnetic components of the FB-FB converter play a more significant role at lower frequencies while the converter volume is more significant at higher frequencies. The magnetic components of the FB-MMC are smaller than the FB-FB configuration although still slightly larger than the MMC-MMC.

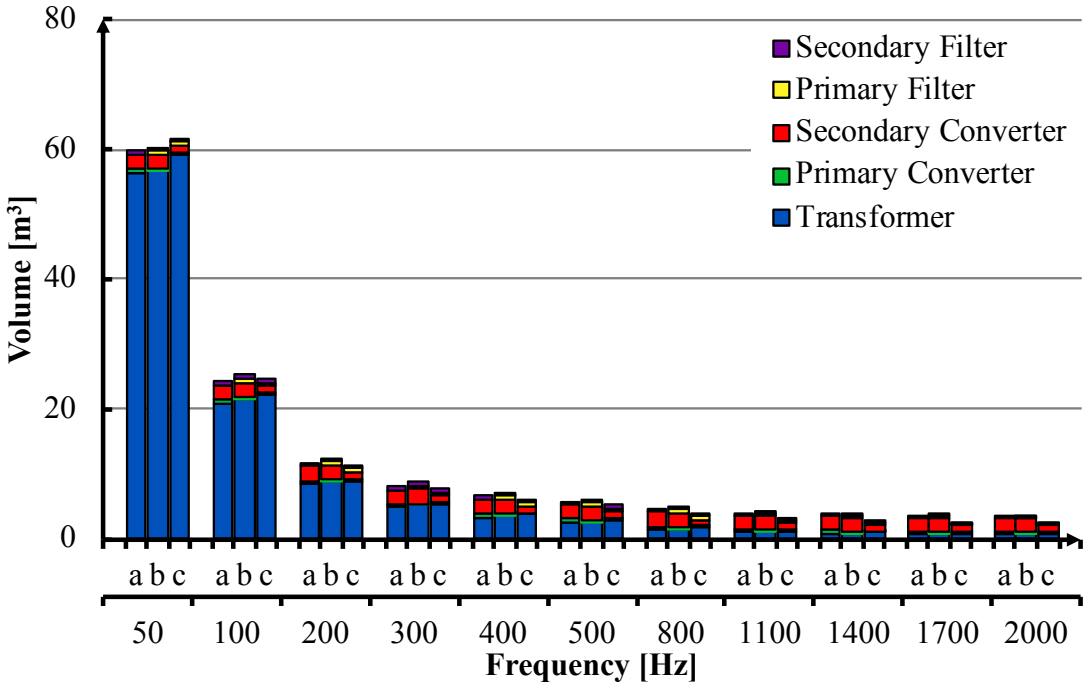


Fig. 3.22 Total transformer volume with 19 turns on the primary winding for the a) MMC-MMC, b) FB-MMC and c) FB-FB converters

The FB-FB configuration provides the smallest volume; however, this is achieved at 2000 Hz where the losses are approaching 60% which is unfeasible. Furthermore, each arm of the secondary converter requires 40 series connected IGBTs to resist the voltage stress. Ensuring each of these switches simultaneously will complicate the design and construction of the converter, increasing its cost. This is solved in the FB-MMC configuration through use of the MMC on the secondary. It also results in a smallest volume over much of the frequency range, however, the primary converter switching losses are twice those of the MMC-MMC. As a result, the MMC-MMC is the preferred topology.

In Fig. 3.23 the total converter losses for the MMC-MMC configuration are plotted against both frequency and the number of primary transformer turns. As can be seen, the converter losses initially reduce rapidly as the number of primary turns increases but then plateaus. As frequency increases, the improvement in efficiency due to increasing the number of primary winding turns decreases. This is because the magnetic component losses generally decrease with frequency while the converter losses increase. As a result, improving the magnetic design has a diminishing effect.

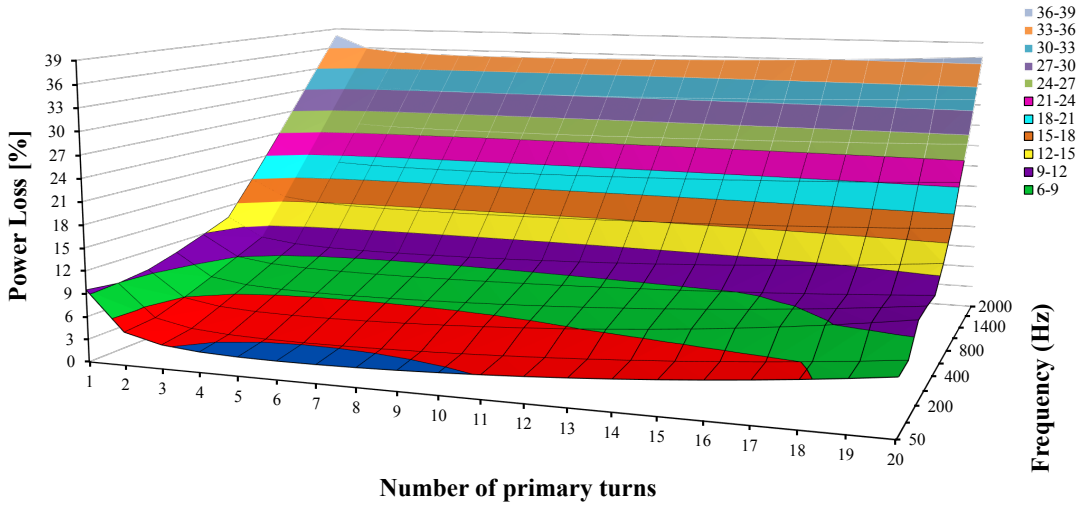


Fig. 3.23 The total MMC-MMC transformer loss for $1 < N_p < 20$ over the MF range as a percentage of the maximum

The effect of increasing the number of primary transformer turns can be seen more clearly in Fig. 3.24. With only 1 turn on the primary, the core area must be very large to prevent core saturation. The core volume is therefore very large and hence dominates the magnetic losses. As the number of turns increases however, the core volume rapidly decreases, reducing its losses. The winding losses begin to increase though, creating an optimum design point of 5 turns on the primary winding.

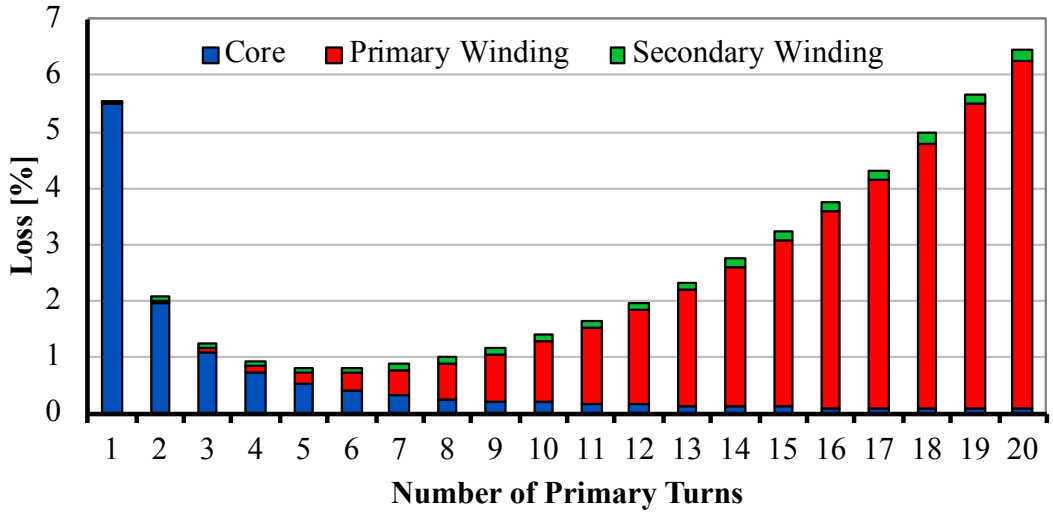


Fig. 3.24 Magnetic transformer losses for the MMC-MMC configuration with $f_0 = 200$ Hz

Looking at Fig. 3.25, the volume initially decreases quickly with both frequency and the number of turns on the primary but soon levels off. When compared to Fig. 3.23, increasing the number of turns on the primary has a more favourable volume reduction to loss increase

ratio compared to increasing the frequency. From these results, the optimum turns on the primary and frequency would appear to be 5 turns at 200 Hz.

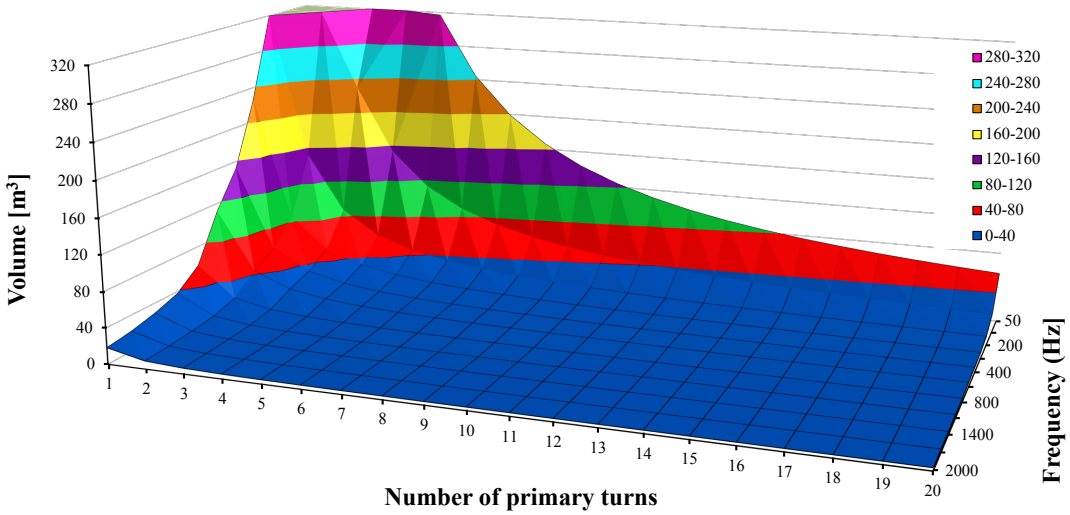


Fig. 3.25 The total MMC-MMC transformer volume for $1 < N_p < 20$ over the MF range

A detailed breakdown of the component losses and volume at the optimal operating conditions is provided in Fig. 3.26. At this operating point, the primary converter accounts for 65% of the total losses, 90% of which are switching losses. This compares to the 77% contribution from the secondary, despite the secondary having 500 switches to the primary's 144. The increase in losses is partially due to the higher primary side current but also the higher switching frequency. It would be beneficial to increase the number of voltage levels on the primary such that the switching loss could be reduced and the filter eliminated, further reducing losses and volume.

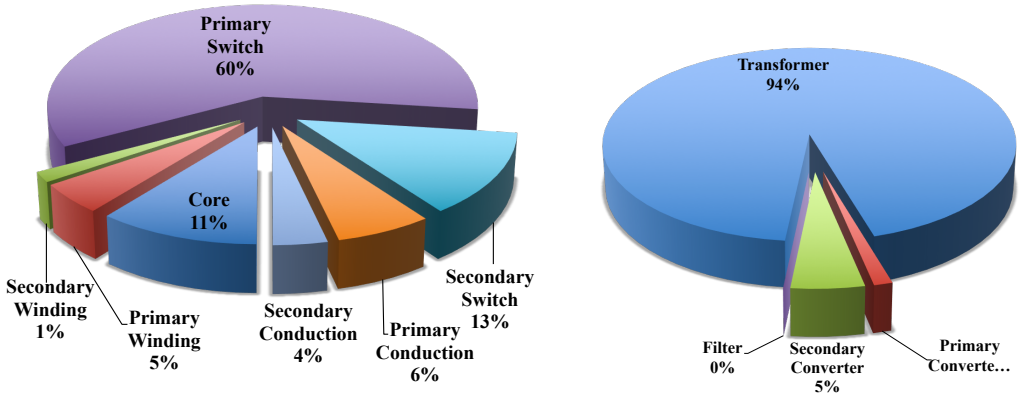


Fig. 3.26 Breakdown of MMC-MMC losses (left) and volume (right) components at $f_0 = 200$ Hz and $N_p = 6$

This would require increasing the number of SMs and hence lead to a higher redundancy on the primary. While this would reduce the chance of converter failure, conduction and switching losses would increase as well as the converter volume and cost due to the added components.

To date, ferrite cores have only been used for low power transformers due to their high expense and poor structural properties (ferrites are very brittle). As such, it would be difficult to design the Hybrid HVDC Transformer around a ferrite core. Interestingly however, the magnetic transformer core loss is low, even towards the top end of the frequency range. As a result, it may be possible and indeed more practical, to use a very thin laminated Iron core instead.

3.6 Chapter Summary

The aim of this chapter was to characterise the accuracies of the FTSE and iGSE and determine the best topology and operating frequency given the unique challenges faced by the Hybrid HVDC Transformer. To accomplish the first aim, the losses predicted by the SE, FTSE and iGSE were compared to those experienced by the Epcos N87 Ferrite core under a selection of operating conditions. This revealed that all three methods were most accurate when the core was excited using a sinusoidal waveform. The accuracy of the FTSE was found to diminish as the *THD* of the flux density increased though, while the iGSE was found to perform best overall, as predicted in the literature.

In accordance with the second chapter aim, mathematical and simulation models of the Hybrid HVDC Transformer's magnetic elements and DC converters were created. These were used to calculate the efficiency and volume of the FB-FB, FB-MMC and MMC-MMC topologies at different operating frequencies and number of primary turns. The transformer efficiency was found to be highly susceptible to switching losses. As such, the PWM carrier frequency should be minimised favouring the MMC-MMC configuration. That said, if the number of voltage levels generated by the primary MMC could be increased, significant improvements in efficiency could be realised.

The key contributions of this chapter are therefore:

- The iGSE is significantly more accurate than the FTSE, particularly for high *THD* flux waveforms
- The Steinmetz parameters for the Epcos N87 core in the 500 – 2000 Hz range are presented in Table 3.2
- The Hybrid HVDC Transformer is highly sensitive the converter switching frequency
- The MMC-MMC topology is therefore preferred however, the operating frequency is still restricted to 200 Hz to constrain the switching losses

- Significant improvements in efficiency can be obtained and higher operating frequencies realised if the number of voltage levels generated by the primary side MMC is increased

A novel control algorithm is therefore proposed in Chapter 4 to increase the number of voltage levels generated for a given MMC. With more voltage levels, the switching frequency of the primary side converter can be reduced and greater efficiencies and operating frequencies realised.

Chapter 4 Conception and Validation of the Proposed High Definition Modular Multilevel Converter

The efficiency of the Hybrid HVDC Transformer was found in Chapter 3 to be very sensitive to the converter switching losses. Therefore, significant improvements in both the its volume and efficiency could be realised by reducing the carrier frequency or using NLM. However, this would increase the filter size or *THD* and negatively affect the control stability and transformer losses. If the number of voltage levels generated by the primary side MMC could be increased however, NLM could be used without these negative effects. The relatively low DC bus voltage restricts the number of voltage levels that can be generated using standard MMC control methodologies though. Techniques to increase the number of MMC voltage levels have been proposed in the literature but are either highly application specific or result in large circulating currents.

The aim of this chapter, is to introduce and validate the High Definition-MMC (HD-MMC) algorithm. The HD-MMC takes advantage of the inherent redundancy present in the MMC to create extra voltage levels and hence does not generate additional circulating currents. Although the HD-MMC was developed for the Hybrid HVDC Transformer, it is valid for any LV or MV application where *THD*, volume or efficiency are of concern. It can therefore offer advantages in grid balancing, Photo Voltaic (PV), wave, tidal, aerospace and Electric Vehicle (EV) applications.

To validate the HD-MMC algorithm, an experiment was conducted using a single-phase, 18 SM MMC at SINTEF's research facilities in Trondheim. The *THD* and number of switching events generated by the HD-MMC were compared to that of a C-MMC using both PWM and NLM. The SM capacitor voltages, arm currents and output voltages were also monitored to ensure the converter operation remained stable.

The objectives of this chapter are therefore:

- The introduction of the HD-MMC control algorithm
- The experimental validation of HD-MMC control algorithm
- Evaluation of the HD-MMC control algorithm compared to the C-MMC using both NLM and PWM
- Introduction of a weighting factor to improve control over the SM balancing process

To achieve these objectives, this chapter is organised as follows; the operating principle and control strategy of the HD-MMC algorithm are explained in Section 4.1. An experimental validation of the proposed HD-MMC algorithm and comparison to a conventional MMC using an 18 SM, single-phase, MMC operated using an open loop control is reported in Section 4.2. Finally, the key findings are summarised in Section 4.3.

4.1 Control Strategy

4.1.1 Operating Principal

The C-MMC switches SMs in and out to generate the desired AC voltage level as described in Fig. 2.8. In a specific cycle, a particular voltage level will be created through a combination of SMs in each arm, the combination of SMs switched in or out forms a state. During the operation of the C-MMC, several different states can be used to generate the same AC voltage level. If more than one state can be used to create a voltage level, each subsequent state is redundant. The redundant states for each voltage level of a C-MMC are highlighted in Fig. 2.8. These redundant states are used by the control algorithm to balance the SM voltages but the large number of them makes inefficient use of the MMC's hardware, increasing the converter's, size cost and losses.

If some of these redundant states are repurposed, the utilisation of the MMC's resources could be improved, thereby realising improvements in performance. The HD-MMC achieves this through charging some of the SM capacitors to a different voltage, as shown in Fig. 4.1. In that example, a conventional 5L MMC with a 10 kV DC bus voltage has been altered such

that two SMs are charged to 2 kV and two to 3 kV. This converter arrangement could therefore be described as having two Sets, a 2 kV Set (U_{S1} = 2 kV) and a 3 kV Set (U_{S2} = 3 kV), with two SMs in Set 1 and Set 2 ($\varsigma_1 = \varsigma_2 = 2$).

SM	Set	u_c	Logic												
		kV	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}
1	1	2	0	1	0	0	1	0	1	1	1	1	0	0	0
2		2	1	1	1	0	0	0	0	1	0	1	1	0	1
3	2	3	0	0	0	0	0	1	1	1	1	1	1	1	0
4		3	1	0	0	0	0	0	0	0	1	1	1	1	1
5	1	2	1	1	1	1	0	0	0	1	0	0	1	0	1
6		2	0	1	0	1	1	0	1	1	1	0	0	0	0
7	2	3	1	1	1	1	1	1	0	0	0	0	0	0	1
8		3	0	0	1	1	1	1	1	0	0	0	0	1	0

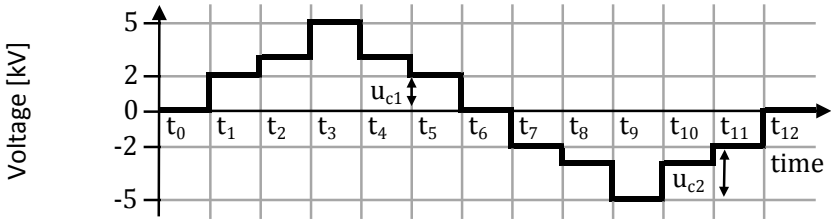


Fig. 4.1 Switching pattern and resulting AC voltage for a 2 Sets with 2 SMs per Set

As can be seen, the four SM converter can now generate nine AC voltage levels (9L) and hence the *THD* of the converter is reduced. In this example, each Set has two SMs ($\varsigma_1 = \varsigma_2 = 2$) and hence there is redundancy within each Set and a standard SM balancing algorithm can be used to maintain the SMs within the Set at equal voltages. There is, however, only one possible Set combination at each time step. For example, at t_1, 1 SM from Set 2 (S_2) is required ($\varsigma_{ON2} = 1$) and at t_2, 1 SM S_1 must be switched on ($\varsigma_{ON1} = 1$). Any other combination at these or any other time steps would result in an irregular waveform. Hence there is no Set redundancy and the voltage of the Sets will diverge from their nominal value until one Set supports the entire DC bus voltage (Fig. 4.2), like a C-MMC in the absence of a SM balancing controller. Set redundancy must therefore be incorporated into the converter design and an additional Set balancing block integrated into the control to administer this.

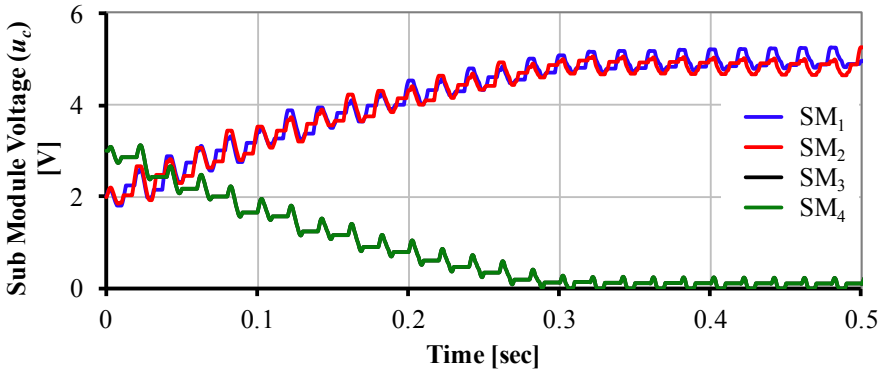


Fig. 4.2 SM voltages over time for a 2 Set, 4 SM converter with no Set redundancy or Set controller

Through careful Set voltage selection, the necessary Set redundancy can be created, allowing a Set controller to balance the voltages. In the proposed HD-MMC this is achieved by ensuring that the potential of a SM (u_{cy}) within the y^{th} Set can be created through the sum of SMs in previous Sets. This gives the maximum voltage of the u_{cy} as:

$$u_{cy} = \sum_{x=1}^{y-1} \varsigma_x \cdot u_{cx} \tag{4.1}$$

This does not leave many redundant Set states however, and so it is recommended that each SM of the y^{th} Set not exceed the sum of voltages in the previous Set giving its voltage as:

$$u_{cy} = \varsigma_{(y-1)} \cdot u_{c(y-1)} \tag{4.2}$$

Selecting the Set voltages in this way also ensures that each voltage step is the same height, reducing the complexity of the Set selection algorithm and minimising the induced harmonics. A diagram of the j^{th} phase of the HD-MMC with g Sets and ς SMs per Set is shown in Fig. 4.3.

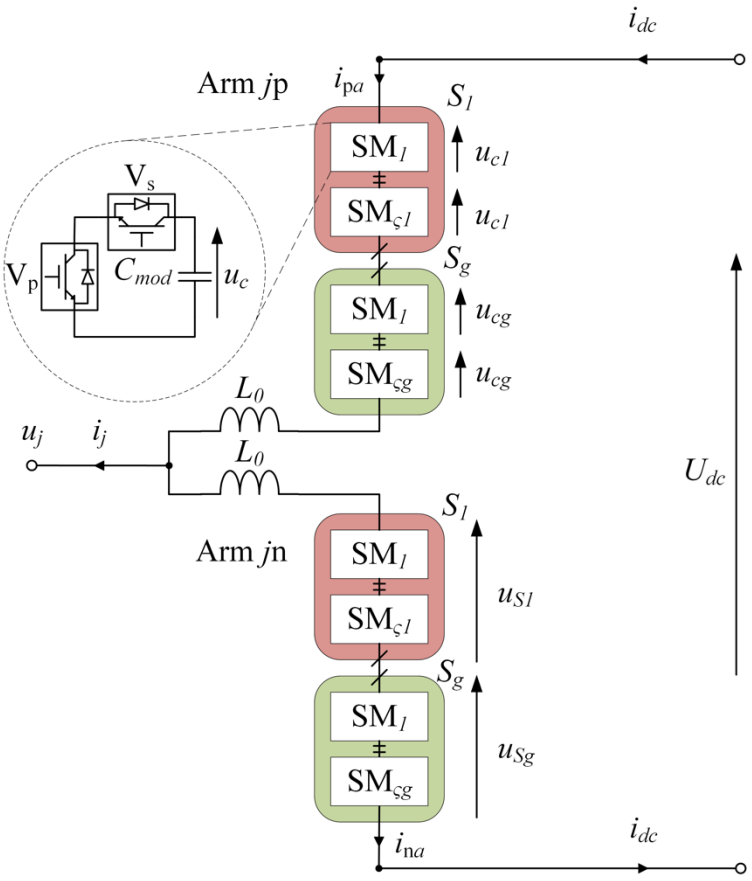


Fig. 4.3 Single-phase circuit diagram of the HD-MMC

The switching states and corresponding AC voltage levels for the HD-MMC assuming (4.2) where $g = 2$ and $\varsigma_1 = \varsigma_2 = 2$ is shown in Fig. 4.4 with the redundant Set states highlighted in green.

SM	u_c [V]	Logic												
		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}
1	u_{c1}	0	1	0	0	1	0	1	1	1	1	0	0	0
2	u_{c1}	1	1	1	0	0	0	0	1	0	1	1	0	1
3	u_{c2} ($2u_{c1}$)	0	0	0	0	0	1	1	1	1	1	1	1	0
4	u_{c2} ($2u_{c1}$)	1	0	0	0	0	0	0	0	1	1	1	1	1
5	u_{c1}	1	1	1	1	0	0	0	1	0	0	1	0	1
6	u_{c1}	0	1	0	1	1	0	1	1	1	0	0	0	0
7	u_{c2} ($2u_{c1}$)	1	1	1	1	1	1	0	0	0	0	0	0	1
8	u_{c2} ($2u_{c1}$)	0	0	1	1	1	1	1	0	0	0	0	1	0

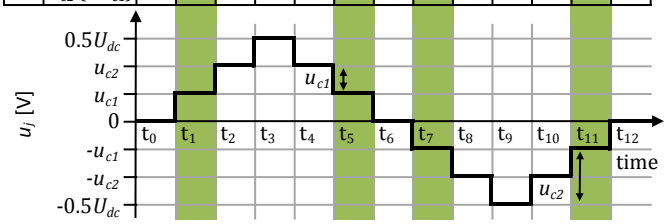


Fig. 4.4 HD-MMC switching pattern

In the first redundant Set state at t_1, the voltage level can be generated by either inserting two SMs from S_1 or one SM from S_2 i.e. $\varsigma_{ON1} = 2$ or $\varsigma_{ON2} = 1$. In this way, there are now four redundant Set states for each cycle compared to none in the example given in Fig. 4.1. It is interesting to note that there are some states in the HD-MMC where there are less than *m* SMs switched in per branch however, since some SMs have higher voltages, the full DC bus voltage is supported and (4.3) is satisfied.

$$U_{dc} = u_{jp} + u_{jn} \tag{4.3}$$

The number of voltage levels that can be created is given by:

$$n = \sum_{y=1}^{g} (\varsigma_y \cdot U_{ry}) + 1 \tag{4.4}$$

Where U_{ry} is the ratio of the y^{th} Set SM voltage to the first Set SM voltage that is to say, $U_{ry} = u_{cy}/u_{c1}$. Using (4.4) the first Set voltage can be defined as:

$$u_{c1} = \frac{U_{dc}}{n-1} \tag{4.5}$$

The number of possible Set states per cycle (n_{st}) can also be calculated from:

$$n_{st} = \prod_{y=1}^{g} (\varsigma_y + 1) \tag{4.6}$$

And hence the number of redundant states (n_{rd}) can be simply defined as

$$n_{rd} = n_{st} - n \tag{4.7}$$

4.1.2 Set Control Algorithm

With redundant Sets, a control algorithm can be developed to balance the Set voltages. Like the SM control, the Set control must use the Set redundancy to balance the Set voltages albeit with an additional condition complicating its design. Since each SM is no longer equivalent, the Set controller must select a SM and Set combination that achieves the desired AC voltage level. Moreover, it should also work in tandem with the SM voltage controller to balance the SM voltages within each Set.

The Set algorithm must select the best Set combination to achieve the desired AC voltage level. First, the available options are determined based on the number of SMs and Sets per arm and each Set's nominal voltage. A matrix containing each of the possible Set combinations

(S_{com}) for each voltage level is pre-populated prior to initiation. An example is shown in Table 4.1 for a 3 Set, $\varsigma_1 = \varsigma_2 = \varsigma_3 = 2$ converter. This can be more concisely written as [2 2 2], where column 1 contains ς_1, column 2 contains ς_2 and column 3 contains ς_2 such that a converter with g Sets is written as $[\varsigma_1\ \varsigma_2\ \ldots\ \varsigma_g]$. When a switching operation is required, the algorithm consults S_{com} to determine the possible Set combinations for the desired voltage level (u_{mod}) set by the modulation control.

Option N°	ς_{ON1}	ς_{ON2}	ς_{ON3}	u_{mod}
1	0	0	0	0
2	1	0	0	1
3	2	0	0	2
4	0	1	0	2
5	1	1	0	3
6	2	1	0	4
7	0	2	0	4
8	1	2	0	5
9	**2**	2	0	6
10	0	0	1	4
11	1	0	1	5
12	**2**	0	1	6
13	**0**	1	1	6
14	1	1	1	7
15	2	1	1	8
16	0	2	1	8
17	1	2	1	9
18	2	2	1	10
19	0	0	2	8
20	1	0	2	9
21	2	0	2	10
22	0	1	2	10
23	1	1	2	11
24	2	1	2	12
25	0	2	2	12
26	1	2	2	13
27	2	2	2	14

Table 4.1 All the Set combinations and corresponding voltage levels for a [2 2 2] converter. The largest Set deviation and required voltage level are highlighted

For most voltage levels, there are multiple possible Set combinations for the algorithm to select from, as shown in Table 4.1 columns highlighted in dark blue. According to (4.5) – (4.6) the redundant states (options) at each voltage level increases with the number of Sets and SMs per Set. Whilst this provides more opportunities to balance the Set voltages, it also complicates the Set selection. For each switching operation, a multivariable optimisation problem is created. In the C-MMC, the SM voltages are balanced by selecting the highest voltage SM when i_{arm} is negative and selecting the lowest voltage SM when i_{arm} is positive, as described in Section 2.1.2. A similar logic can be applied here if a normalised, relative voltage deviation ΔU_{Sy} is calculated for each Set as in:

$$\Delta U_{Sy} = \frac{(u_{Sy} - U_{Sy})}{U_{Sy}} \times 100 \tag{4.8}$$

Where U_{Sy} is the nominal voltage for the y^{th} Set and is calculated from:

$$U_{sy} = \frac{U_{dc}}{m} \varsigma_y \cdot U_{ry} \tag{4.9}$$

The C-MMC balancing algorithm could then be altered for Set balancing in two different ways:

1. If $i_{arm} > 0$ choose the option that inserts the maximum number of SMs from the Set with the lowest ΔU_{Sy}. If $i_{arm} < 0$ choose the option that inserts the maximum number of SMs from the Set with the highest ΔU_{Sy}.
2. Find the Set with the largest $|\Delta U_{Sy}|$ and if $i_{arm} < 0$ and $\Delta U_{Sy} > 0$ then choose the option with the highest number of SMs switched in from this Set, if $i_{arm} > 0$ and $\Delta U_{Sy} > 0$ choose the option with the least number of SMs switched in from this Set. If $i_{arm} < 0$ the inverse is true.

Other options are possible; however, they only consider the optimum solution for 1 Set. This is acceptable if there are only two Sets. For example, charging the first Set will discharge the second and vice versa. This relationship is more complicated for converters with more than two Sets though. Single variable optimisations are unlikely to result in the best selection resulting in large voltage deviations at some modulation indexes (Fig. 4.5). This is explained in Section 5.2.

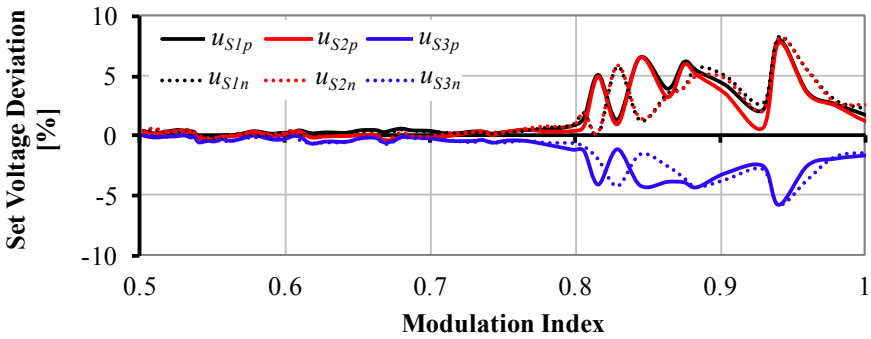


Fig. 4.5 Excessive Set voltage deviation in a [4 4 4] converter caused by single variable optimisation in the Set voltage balancing algorithm

This can be further exemplified through use of Table 4.1. Take $u_{mod} = 6$, there are 3 options as shown in Table 4.2.

Option	ς_{ON1}	ς_{ON2}	ς_{ON3}	u_{mod}
9	2	2	0	6
12	2	0	1	6
13	0	1	1	6

Table 4.2 Set combinations capable of creating a voltage level of U_{ref} = 6 for a [2 2 2] converter.

If it is assumed that i_{arm} is positive for both u_{mod} = 6 and u_{mod} = 5 and that $\Delta U_{S1} = 2\%$, $\Delta U_{S2} = 1\%$ and $\Delta U_{S3} = -1\%$ then the first single variable optimisation option would determine options 12 and 13 to be equally suitable. The second single variable optimisation would determine options 9 and 12 as both being good options. Logically, option 13 is significantly better than the alternatives as it charges the two lowest voltage Sets (S_1 and S_3) while not influencing the highest voltage Set (S_1).

It is therefore important to consider the best overall configuration, not just the best for one Set. The optimal overall configuration can be most aptly described as the one that results in the smallest overall Set deviation over the next time step. From this definition, the desired configuration can be found by finding the error for the i_o^{th} option, $\epsilon_{op\,i_0}$.

$$\epsilon_{op_{i_o}} = \sum_{y=1}^{g} \Delta U_{s_y} \varsigma_{ONy} \tag{4.10}$$

If $i_{arm} > 0$ the option with the lowest error is considered the optimal Set configuration, otherwise, if $i_{arm} < 0$, the option with the highest error value is selected. In converter configurations with large numbers of Sets it is possible that two or more options will have the same error. In this case, the algorithm chooses the option that requires the least switching operations to minimise converter losses. This is determined by comparing the number of SMs required in each Set to the SMs already on for each option. A high-level flow diagram of the Set control algorithm is shown in Fig. 4.6.

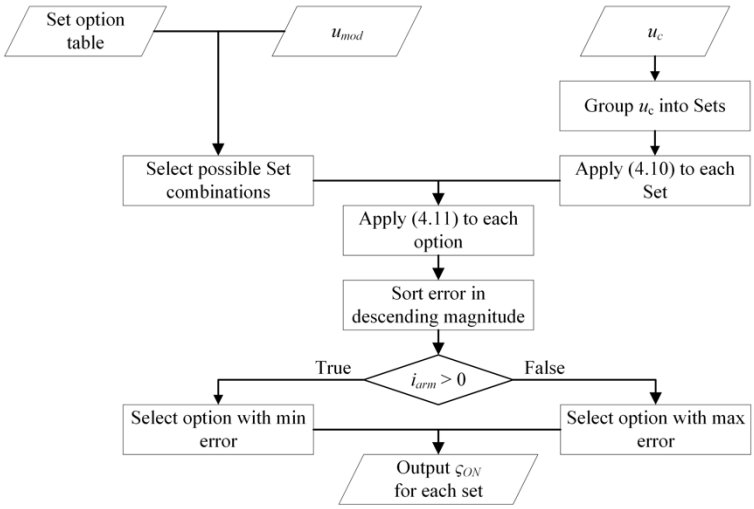


Fig. 4.6 A flow diagram of the Set voltage controller

Using the same example described for the single variable optimisations, options 9, 12 and 13 would be identified as possibilities to generate $u_{mod} = 6$, as highlighted in Table 4.1. From this, the option error can be calculated as

$$\epsilon_{op_9} = 2 \cdot 2\,\% + 2 \cdot 1\,\% + 0 \times -1\,\% = 6\,\%$$
$$\epsilon_{op_{12}} = 2 \cdot 2\,\% + 0 \cdot 1\,\% + 1 \cdot -1\,\% = 3\,\%$$
$$\epsilon_{op_{13}} = 0 \cdot 2\,\% + 1 \cdot 1\,\% + 1 \cdot -1\,\% = 0\,\%$$

If $i_{arm} > 0$, the option 13 would be chosen as it has the lowest error, if however, $i_{arm} < 0$, option 9 would be selected. If two of the options had the same error, the algorithm would then compare the total number of switching operations required for each and choose the option that had the least. By using this approach, the Set deviation for a [4 4 4] converter can be reduced from Fig. 4.5, to that shown in Fig. 4.7.

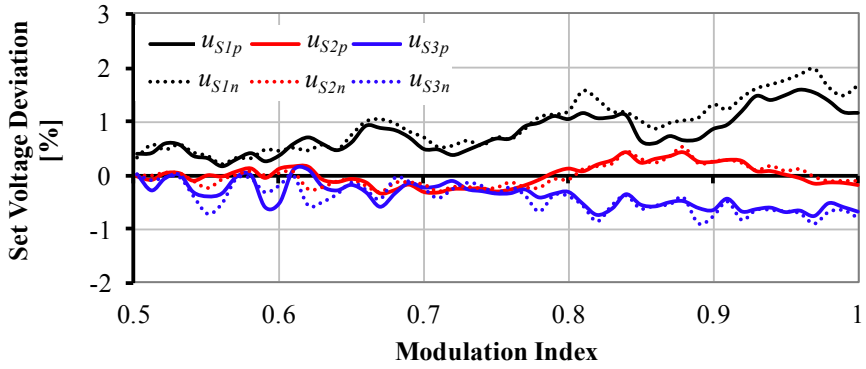


Fig. 4.7 Set voltage deviation in a [4 4 4] converter as a result of the Set voltage balancing algorithm using multivariable optimisation

4.1.1 Power and circulating current control algorithms

The Set controller changes the operation of the MMC. Given this, the mathematical analysis of the C-MMC's operation described in Section 2.1.3 may not be applicable to the HD-MMC, throwing into question the viability of existing power, current and circulating current control. The assumptions used to derive these algorithms are therefore re-assessed for the HD-MMC below.

The fundamentals of the power and current controllers assume that the arm SMs of the MMC can be replaced by a sinusoidal voltage source, the accuracy of which is improved as more voltage levels are created. As the circuitry of the HD-MMC and end goal of the control (i.e. to generate a sinusoidal waveform) remains unchanged, this assumption remains valid. It could be argued that since the HD-MMC creates additional voltage levels, the arm SMs more closely approximate a sinusoidal voltage source in the HD-MMC, especially with few voltage SMs.

The circulating current analysis is more complicated though, since, while the structure and goal of the HD-MMC remains the same as the C-MMC, the execution differs. From Fig. 4.8, it can be seen that the number of SMs inserted no longer follows a simple sinusoidal pattern and the analysis performed in [93] is not valid. A different approach is therefore required. In [91] the power stored in the SM capacitors is calculated based on the arm voltage and current which shows there must be a double line frequency and DC component in the sum of the arm voltages. Since this analysis assumes that the arm SMs can be replaced by a sinusoidal voltage source it is still valid. A second order harmonic is therefore still present and the derivation of the CCS in Section 2.1.3.2 remains applicable.

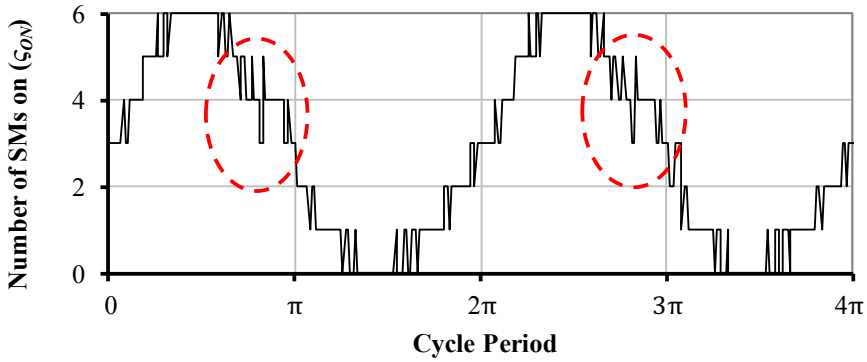


Fig. 4.8 The number of SMs switched on over the period of 4 cycles. The red ovals highlight areas where the waveform differs from its usual sinusoidal form

The high-level control functions used in the C-MMC can therefore be used to control the HD-MMC. Given this, it would be beneficial if the application of the Set controller was minimally

invasive and applicable to different control topologies. This will maximise its applicability to industry and simplify its implementation. The Set controller has therefore been designed to sit within the existing control structure (Fig. 4.9), intercepting and translating the modulation signals for the SM controller to generate the required gate signals to realise the HD-MMC concept.

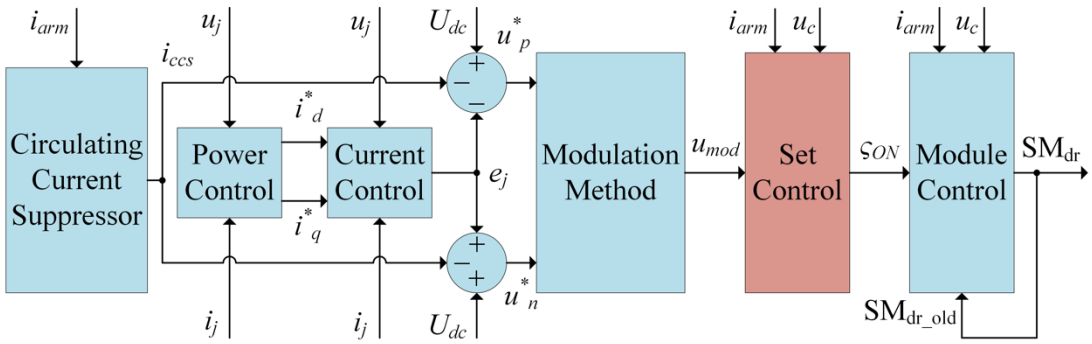


Fig. 4.9 Overview of the HD-MMC control strategy. The modification to the control strategy of a HB-MMC is highlighted

4.1.2 SM balancing algorithm with weighting factor

As discussed in Section 2.1.2, it is possible to significantly reduce (by up to 75%) the switching losses of the converter by using a reduced switching frequency algorithm. This is highly advantageous especially at higher fundamental frequencies as switching losses become more dominant. By reducing the switching frequency though, the capacitor voltage ripple increases, which, in turn, negatively influences the SM capacitor life, control stability and converter *THD*. These effects, can be mitigated by increasing the SM capacitance but this will influence the size and cost of the converter.

Given the importance switching frequency has on the converter behaviour, it would be useful to have greater control over it rather than merely the maximum (conventional control) or minimum (reduced switching frequency) options listed in Section 2.1.2. For this reason, a SM balancing algorithm incorporating a weighting factor was developed in collaboration with SINTEF and is described here.

In the reduced frequency method, SMs are excluded from the sorting process if they are already switched in or switched out when an additional SM is to be switched in or out respectively. As a result, there is only one switching event per arm at each change in voltage level. In the proposed SM balancing algorithm, a weighting factor (k_w) is introduced that

allows the user to define the importance that the SM's current state has when sorting. This weighting factor is used to create a revised SM voltage (u_c') according to (4.11) before being sorted.

$$\begin{aligned} u_c' &= u_c - k_w \cdot U_c \cdot \eta_m, \qquad i_{arm} > 0 \\ u_c' &= u_c + k_w \cdot U_c \cdot \eta_m, \qquad i_{arm} < 0 \end{aligned} \tag{4.11}$$

The weighting factor is specified as a percentage of U_c, such that one factor can be specified for all Sets and is multiplied by the SM's current state ($\eta_m = 1$ or $\eta_m = 0$). Then, the revised SM voltages can be sorted and the required number of SMs selected from the top of the pile if $i_{arm} < 0$ or the bottom if $i_{arm} > 0$. A high-level flow diagram of the SM balancing algorithm used in this chapter is shown in Fig. 4.10.

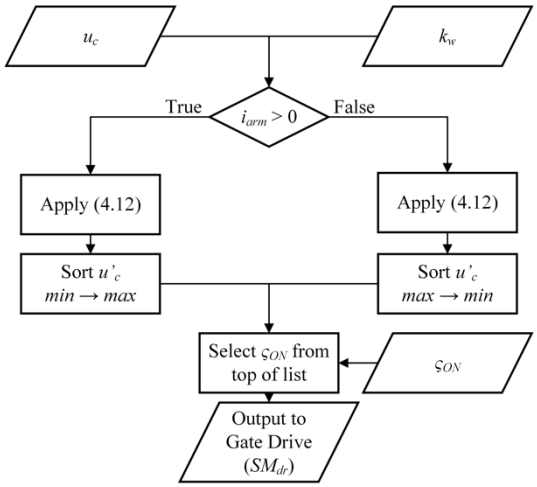


Fig. 4.10 A high level flow diagram of the SM balancing algorithm used

4.2 Experimental Validation of the HD-MMC Algorithm

This section covers the method, experiment Set-up and results of the validation of the HD-MMC algorithm covered in Section 4.1. In addition to verifying its correct operation, the efficiency and *THD* generated by the HD-MMC was also compared to a conventional MMC using both NLM and PWM. Prior to the experiment several simulations were run to verify the proposed experiment set-up and determine which cases to run in the MMC test facility. The experiments were run in collaboration with SINTEF, Norway whose facilities were used in the experiment and IREC, Spain who acted as an independent invigilator.

4.2.1 Experiment Methodology

The experiment had 3 main objectives:

1. Demonstrate the correct operation of the HD-MMC algorithm
2. Quantify the impact of the weighting factor
3. Evaluate the performance of the HD-MMC algorithm compared to a C-MMC using NLM and PWM

To operate correctly, the HD-MMC algorithm must create the number of voltage levels specified by maintaining stable Set voltages at the prescribed values and selecting the correct Set combinations. As a result, each arm voltage should be equal and 180^o out phase with the required number of voltage levels. The upper and lower arm voltages should also always equal U_{dc} such that the circulating current is restricted to the second order harmonic without any fundamental component. Furthermore, the second order harmonic should not escape the converter such that the current at the AC terminal is at the fundamental frequency. The AC terminal current should also be the sum of the fundamental currents of both the upper and lower arms. For this to occur the Set voltages should be well balanced and remain at the prescribed values. These requirements can all be easily verified by measuring the arm voltages and currents, SM voltages and output current.

As described in Section 4.1 the purpose of the weighting factor is to provide an easy and dynamic method to move between the minimum switching case to maximum switching case. This is evaluated by running the MMC under three different weighting factors, a minimum, middle and large value and counting the number of switching events for each case.

The purpose of the HD-MMC algorithm is to provide a more efficient method to reduce the converter *THD* compared to PWM. Therefore, to assess its performance, the *THD* and efficiency were measured for 3 converter control methods:

1. Conventional MMC using NLM
2. Conventional MMC using PWM
3. HD-MMC using NLM

As the SMs in S_2 increases, the number of levels generated will also increase however, the redundant states available will decrease. The Set voltages could therefore become less stable and have a negative impact on the converter performance. Therefore, three Set combinations were tested for the HD-MMC, [9 9], [5 13] and [3 15].

While the converter efficiency was calculated by comparison of the input and output power, it is unlikely to provide a useful comparison. Due to the designed power and voltage rating of the MMC at SINTEF, MOSFET switches were used in place of the more common IGBT for higher power applications. The function of the MMC is unaffected by this but MOSFET

switching losses are significantly lower than those of the IGBT. Since the main difference between each control method is the switching frequency, the difference in efficiency will be very small and hard to measure. A more practical method to compare efficiencies is therefore to count the number of switching events that occur per cycle. Since the conduction losses should be roughly equal among the control methods, the number of switching events are proportional to the converter efficiency. Moreover, the number of switching events will be the same for each specific control method, regardless of the switching device used so the results can be more widely interpreted.

To accomplish each of the three objectives, 15 cases will be run, each with a different combination of modulation method, weighting factor and Set structure as shown in Table 4.3.

Case N°	Modulation Method	k_w	Structure	n
1	NLM	0	[18 0]	19
2	NLM	500	[18 0]	19
3	NLM	5000	[18 0]	19
4	PWM	0	[18 0]	19
5	PWM	500	[18 0]	19
6	PWM	5000	[18 0]	19
7	NLM	0	[9 9]	28
8	NLM	500	[9 9]	28
9	NLM	5000	[9 9]	28
10	NLM	0	[5 13]	32
11	NLM	500	[5 13]	32
12	NLM	5000	[5 13]	32
13	NLM	0	[3 15]	34
14	NLM	500	[3 15]	34
15	NLM	5000	[3 15]	34

Table 4.3 Details for each experiment and corresponding case number

4.2.2 Experiment Set-up

To minimise any external influence on the results and focus the analysis on the HD-MMC algorithm alone, the experiments were conducted on a single-phase, 19L MMC. The converter was run in open loop without any power or circulating current control (high level control). This is the most basic representation of the MMC and as such, the only factor that could influence the results, was the HD-MMC algorithm. The compromise for using this approach is that it does not represent a typical case and so the real-life application of the HD-MMC is not tested. This will be covered through simulations in Section 5.1 and through further experiments planned for November 2017 to be run by a consortium of ORE Catapult, SINTEF, Technalia and IREC.

As the MMC was run in open loop, a passive Resistive Inductive load (RL) load was connected to the AC terminal of the converter as shown in Fig. 4.11.

Fig. 4.11 Passive inductive (left) and resistive (right) loads connected to the AC terminal of the MMC

The power was supplied to the DC bus through a 3-phase diode rectifier via an autotransformer with a variable output voltage (Fig. 4.12) and smoothed by the DC capacitors shown in Fig. 4.13.

Fig. 4.12 Diode rectifier and autotransformer used to supply the DC link voltage for the MMC

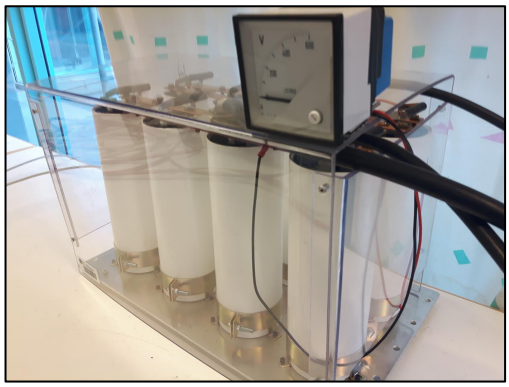


Fig. 4.13 DC link capacitors used to smooth DC link voltage after diode rectifier.

The DC bus was then connected to the DC terminals of the MMC used to experimentally validate the HD-MMC concept. SINTEF have custom built three, 60 kVA, MMC topologies, including a six SM half bridge, 12 SM full bridge and an 18 SM half bridge to provide a rapid testing environment for novel converter and DC grid control strategies. To demonstrate the HD-MMC control algorithm, the 18 SM converter was used in single-phase. A summary of the experiment set- up is illustrated in Fig. 4.14 and the main converter ratings are given in Table 4.4.

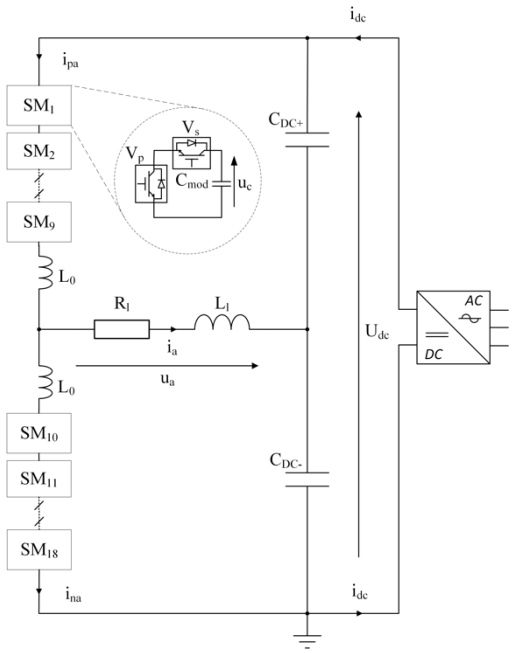


Fig. 4.14 Experiment set-up using single-phase MMC with 18 SMs and an RL load

Parameter	Symbol	Value
Rated power	S	60 kVA
DC link voltage	U_{dc}	776 V
No. of SMs per arm	m	18
SM capacitance	C_{mod}	19.8 mF
Arm inductance	L_0	1.5 mH
Load resistance	R_l	3.2 Ω
Load inductance	L_l	33 mH
DC link capacitance	C_{dc}	19.8 mF
Operating frequency	f_0	50 Hz
Sampling frequency	f_S	10 kHz

Table 4.4 Rated values for the MMC used for the experiment

Each MMC is constructed of several custom-built power cells as shown in Fig. 4.15 each housing two SMs with the SM capacitance, MOSFETS, voltage and temperature sensors as well as the gate drive. These are then assembled into cells with three to four power boards within each cell (Fig. 4.16), which can then be stacked together to form a converter within a cabinet (Fig. 4.17).

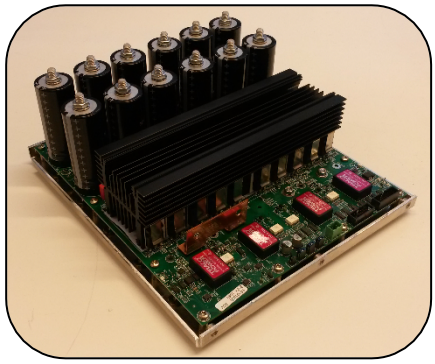


Fig. 4.15 A power cell housing: two MMC SMs including SM capacitor, MOSFETS, sensors, gate control and heat sink

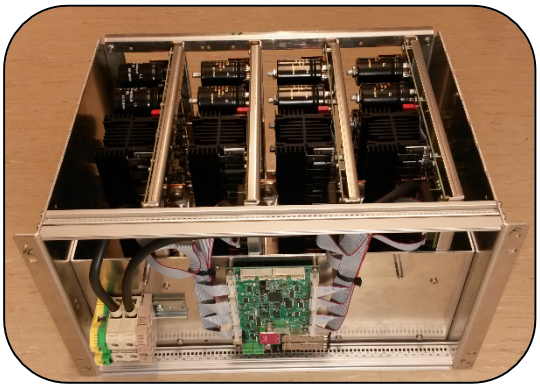


Fig. 4.16 A MMC cell containing 4 power boards

Fig. 4.17 Stacked power boards within cabinet including the switchgear, arm inductors and power cells

A hierarchal approach is taken to controlling each of the MMC converters as shown in Fig. 4.18. The high-level control functions are run from a Simulink file with has a real-time link to the central control board via Opal-RT and a fibre-optic link. This is a two-way communication and measurements from the SMs are used to inform the control and can be displayed in Simulink in real-time.

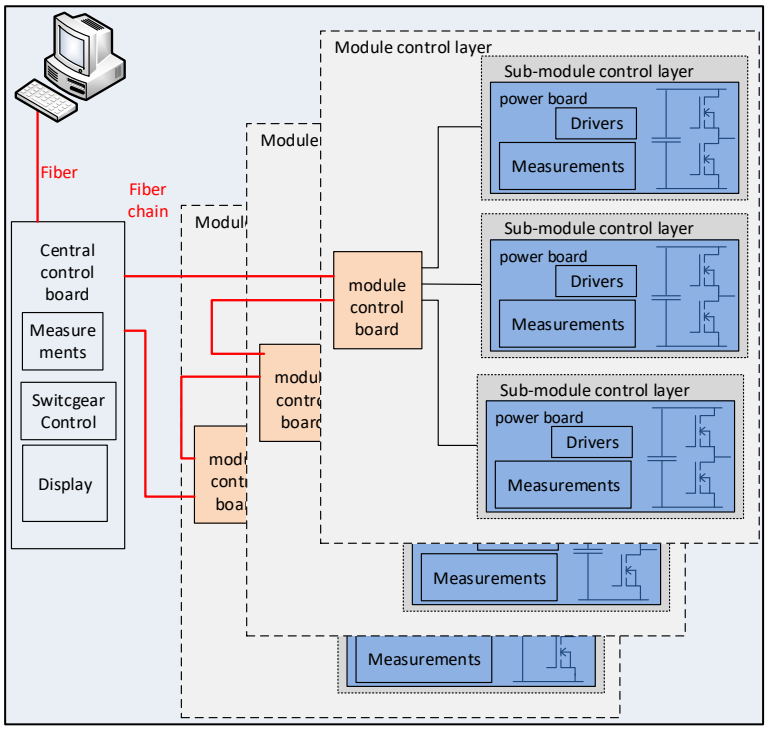


Fig. 4.18 Hierarchal control structure created for the MMCs at SINTEF

The central control layer (Fig. 4.19) is responsible for the converter and AC switch gear control as well as the voltage measurements (i.e. both AC and DC), arm currents from the converter. This layer is controlled by the PicoZed7030 system on chip with two independent ARM-A9 processors and a Field Programmable Gate Array (FPGA) collectively referred to here as the central control board. This is also where the eight channel, 40 MHz, Analogue to Digital (A/D) converter is housed allowing high oversampling rates.

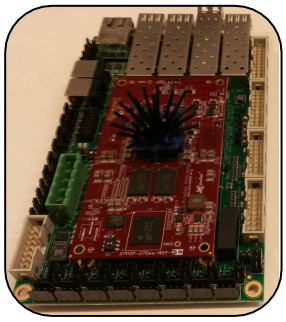


Fig. 4.19 MMC central control board

The converter cells are governed by a group control board (Fig. 4.20) mounted on each of the cells receiving its instructions from the central control board via a fibre-optic. This is operated in a chain structure based on the Aurora point to point protocol developed by Xilinx with a 3.75 Gbit/s bit rate and is used to synchronise each of the power boards.

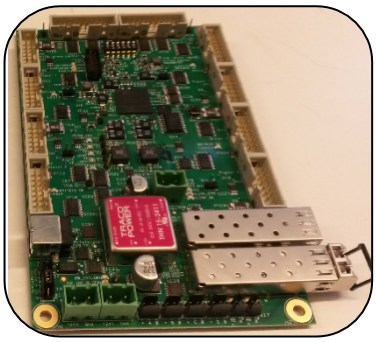


Fig. 4.20 Group control board

The group control board itself controls the three to four power boards within the Set, sending the signals to the gate drivers, gathering the sensor data and status signals of each SM. The board is powered by a Xilinx Artix XC7A35T FPGA with soft embedded processor. Each of the power boards also has an inbuilt control concerned with the basic interlock and protection functions.

4.2.3 Results

Each case detailed in Table 4.3 was run using the single-phase open loop MMC shown in Fig. 4.14. The purpose of the experiments as specified in Section 4.2.1, was to: demonstrate the correct operation of the HD-MMC; quantify the impact of the weighting factor; and evaluate the performance of the HD-MMC against a C-MMC using NLM and PWM.

To operate properly, the HD-MMC must generate the prescribed number of voltage levels. The arm current should be composed predominantly of the first and second harmonic and the SM capacitor voltages must remain balanced and stable.

To demonstrate this, two cases were chosen, one from the conventional MMC (case 2) as the control and the second from the HD-MMC (case 11) to be investigated. In both cases, NLM and the middle weighting factor (k_w = 500) are used to enable a fair comparison. The resulting waveforms are shown in Fig. 4.21 to Fig. 4.26 in per unit form with the same base.

A 50 Hz, 19L sinewave is generated by the upper and lower arms with an 180^o phase shift in the conventional MMC (Fig. 4.21) as expected. It can be seen that some steps lack clarity due to some high frequency switching events. This is also present on the HD-MMC case, as illustrated in Fig. 4.22; however, the resolution is improved. The magnitude of the arm voltages are also marginally lower than those of the C-MMC.

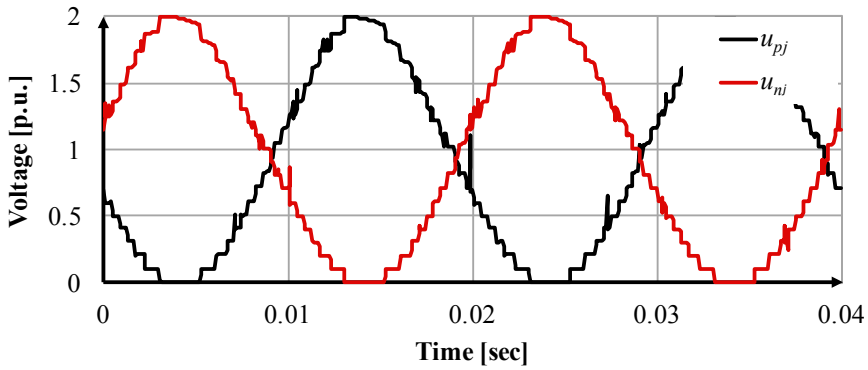


Fig. 4.21 Upper and lower arm voltages (u_{pj} and u_{nj}) of case 2

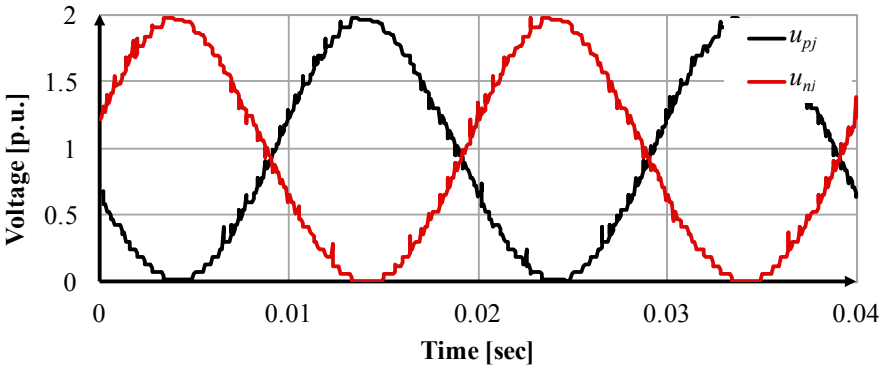


Fig. 4.22 Upper and lower arm voltages (u_{pj} and u_{nj}) of case 11

The upper arm currents of both case 2 and 11 are displayed in Fig. 4.23. While the frequency and phase for both cases are the same, the peak current is higher in case 2. Both cases contain a very large second harmonic component (Fig. 4.24) which would ordinarily be cancelled with a circulating current suppressor in the high-level control. The second harmonic is also larger in case two which is the main contributor to the increased arm current (Fig. 4.23). However, this second harmonic current is not present through the load (Fig. 4.25). Only the load current for case 11 is shown here for clarity as it is identical for both cases. Capacitor waveforms from six SMs in both cases are shown Fig. 4.26. In case 11, the SMs chosen are split evenly between the two Sets (three per Set). The voltage ripple for both Sets is at least comparable to that of case two with the voltage ripple of S_1 being significantly lower. From Fig. 4.26, the mean value of S_1 is 0.06 p.u. exactly half of S_2 at 0.12 p.u.

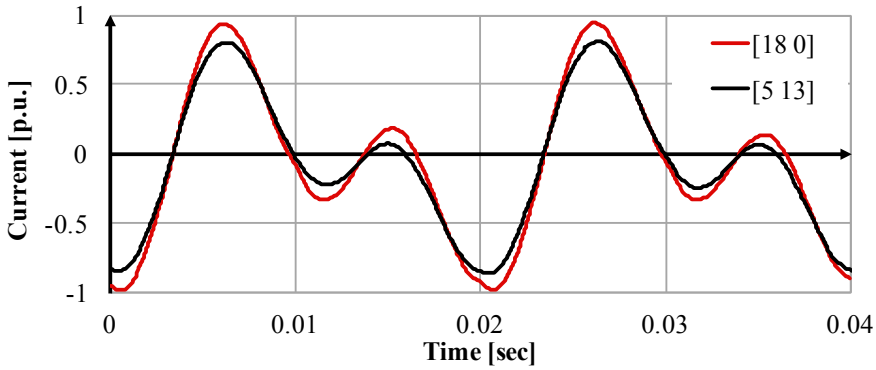


Fig. 4.23 Upper arm currents of cases 2 and 11

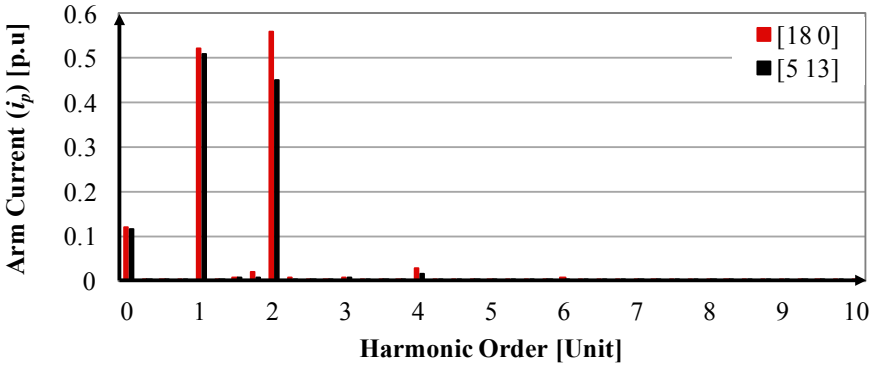


Fig. 4.24 FFT of the upper arm current for cases 2 and 11

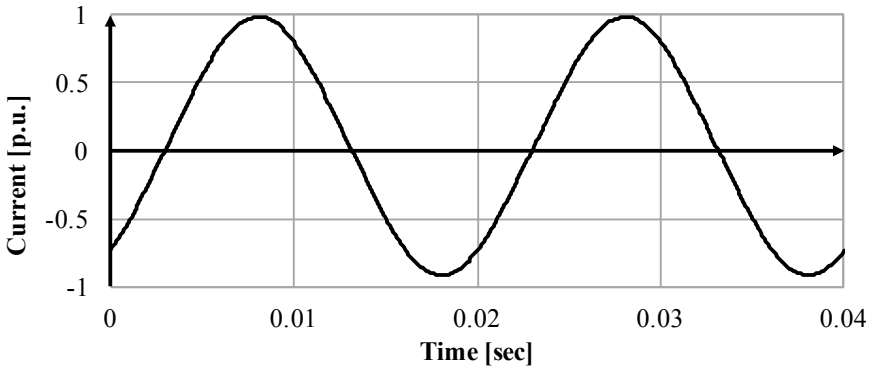


Fig. 4.25 Load current of case 11

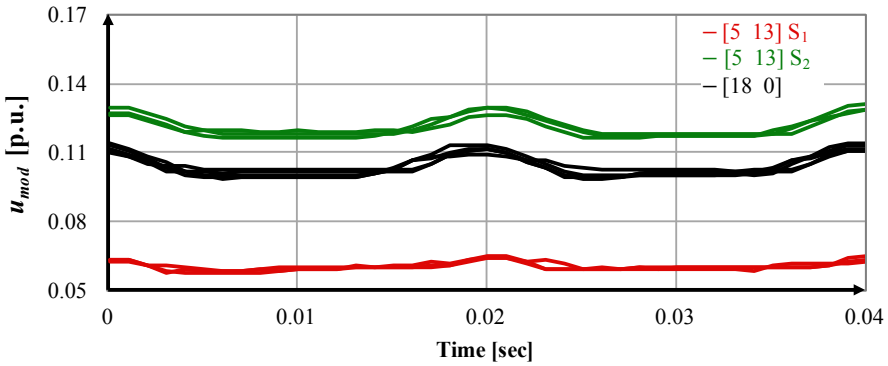


Fig. 4.26 Six SM capacitor (u_c) waveforms for cases 2 and 11

The number of switching events per case, grouped by weighting factor, Set topology and modulation strategy is shown in Fig. 4.27. While the modulation strategy has the largest impact on the number of switching events, the weighting factor has an influence too. As the weighting factor increases, its additional impact diminishes for each case. It has the greatest influence on the conventional MMC with NLM with the number of switching events decreasing from 33k to 8.5k after the first iteration. This is compared to 30.6k to 12.3k in the NLM [9 9] $k_w = 0$ case where the number of switching events is lower than the equivalent conventional topology. The number of switching events increases with the number of SMs in the second Set for a given modulation strategy and k_w value. Furthermore, the rate of this rise increases as the number of SMs in S_2 rises.

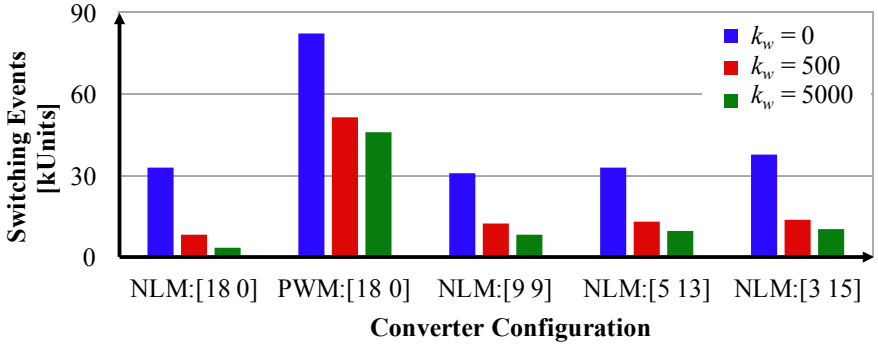


Fig. 4.27 A plot of the number of switching operations for each case tested.

A summary of the key results can be viewed Fig. 4.28 where the *THD* for each case is plotted against the number of switching events. Each case is plotted using its listed reference in Table 4.3, with different colours used for each Set and modulation strategy configuration for clarity. The optimum converter operating point is in the bottom left corner where the minimum switching events and *THD* occurs.

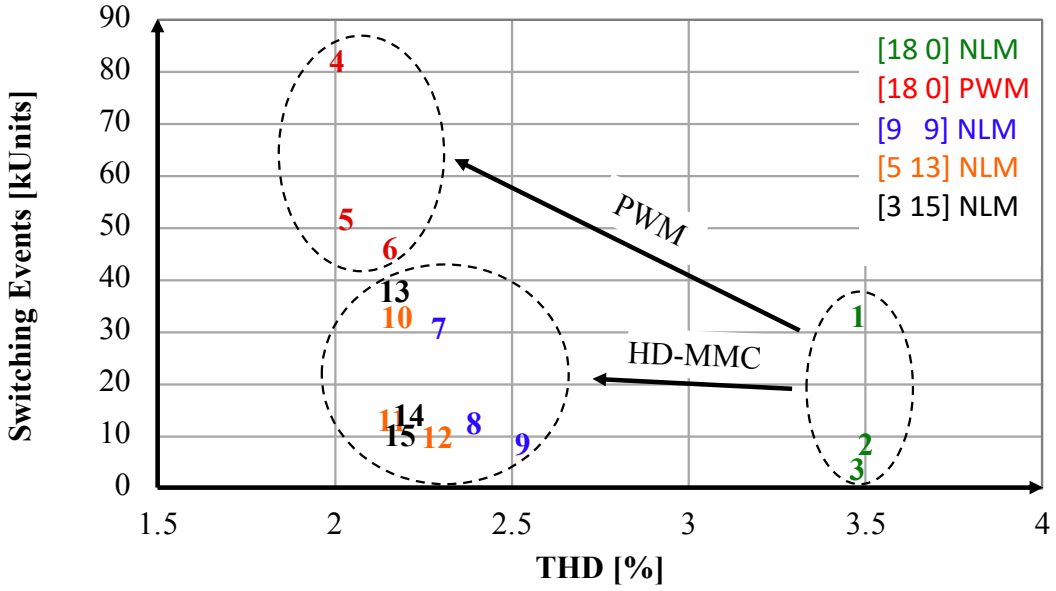


Fig. 4.28 Summary plot showing the Total Harmonic Distortion vs. the number of switching events

While it was noted that the switching frequency would yield a better indication of the converter losses for each configuration, the measured losses are displayed in Fig. 4.29. Care should be taken when interpreting these as there is likely a large degree of uncertainty around them.

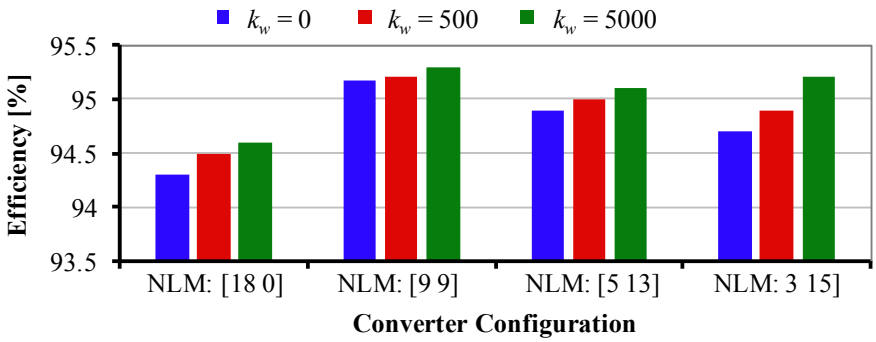


Fig. 4.29 Converter efficiencies for each Set configuration at 3 different weighting factors

Nonetheless, they do show that increasing the weighting factor does improve the efficiency and surprisingly that the HD-MMC is more efficient than the C-MMC despite the higher switching frequency.

4.2.4 Discussion

In converters, there is always a switching delay from when the gate drive receives the turn off or on signal to when the switch is fully blocked or turns on. Since it is vital that the both valves in the SM (V_s and V_p) (Fig. 2.7) are not allowed to both conduct simultaneously, a control delay is used to ensure one switch turns off before the other turns on. The result of this delay can be seen in the voltage spikes present in Fig. 4.21 and Fig. 4.22, where each SM is not switched simultaneously. Additional noise is also present due to the switching in of partially charge or overcharge SMs. The control updates the SMs to be switched in at every time step which can create many of these voltage spikes, particularly when the weighting factor is low. At low weighting factors, the switching frequency increases as no preference is given to SMs already switched in when the SMs are sorted according to their state of charge. The voltage imbalance of the SM capacitors is therefore reduced which can lead to an improved *THD* as in cases 2 – 4. The magnitude and frequency of the voltage spikes caused by the switching delay is largest at lower weighting factor values and may explain why in cases 1 and 5 the *THD* improves as the weighting factor increases.

The higher efficiencies of the HD-MMC configurations compared to the C-MMC can be explained by considering the arm harmonics of each case. It is known from Fig. 4.24 that the largest arm harmonics occur in the C-MMC cases, with the largest difference between the two cases occurring at the second harmonic. These harmonics contribute to the converter losses and help explain why the HD-MMC configurations are more efficient than the C-MMC. In a realistic case however, the second harmonic would be suppressed. Since this accounts for the greatest difference in the harmonics between each case, the C-MMC would likely become more efficient than the HD-MMC.

While it is not surprising that increasing the number of voltage levels gradually produces smaller returns in terms of *THD* reduction, it is still expected to improve. In some instances, however, the [5 13] case has a lower *THD* than the [3 15] case for the same weighting factor, even though the [3 15] case generates an additional two voltage levels. This could be due to the [3 15] case generating a larger Set voltage error and hence generating additional harmonics. If this is the case, this could suggest that there is a lower limit to the number of SMs in each Set which is investigated thoroughly in Section 5.2.

4.3 Chapter Summary

The aim of this chapter was to introduce and validate the High Definition-MMC (HD-MMC) algorithm which was developed to increase the number of voltage levels generated by the primary side MMC. As a result, the operating frequency can be increased, efficiency improved and volume reduced. While the HD-MMC was developed for the Hybrid HVDC Transformer, it can benefit a variety of LV and MV applications where efficiency, *THD* and volume are considerations.

By repurposing some redundant states and grouping the SMs within each arm into Sets, the HD-MMC algorithm creates extra voltage levels without generating additional circulating currents. This was verified experimentally using the single-phase, 18 SM MMC operated in open loop at SINTEF's research facilities in Trondheim. Three, HD-MMC configurations were tested, including a [9 9], [5 13] and [3 15] and then compared to an 18 SM C-MMC using NLM and PWM. The measured SM voltages from each Set showed that the HD-MMC algorithm balanced SM voltages, crucial in providing a stable converter output. The *THD* produced by the HD-MMC was shown to be similar to that of the C-MMC using PWM (2.2% vs. 2.1%) and significantly lower than the C-MMC using NLM. While the HD-MMC algorithm did increase the number of switching events compared to the C-MMC using NLM, it was significantly lower than that of the C-MMC using PWM. Hence the HD-MMC algorithm may be a promising alternative to the use of PWM in some applications.

The key contributions of this chapter can therefore be summarised as:

- The introduction of the HD-MMC's operating principles
- Experimental validation of the HD-MMC algorithm, demonstrating its benefits over PWM for LV and MV applications.
- The introduction of a weighting factor to improve control over the SM voltage balancing algorithm
- Experimental validation of the weighting factor

Chapter 5 **Operating Envelope of the HD-MMC**

The operating principle and experimental validation of the HD-MMC using single-phase and open loop control were discussed in Chapter 4. The HD-MMC should also be validated in 3-phases using a closed loop control to represent a more realistic situation. The operating envelope of the HD-MMC algorithm must also be explored and clearly defined to identify any limitations so that they can be addressed.

To that end, the aim of this chapter is to verify the HD-MMC under realistic running conditions and define its operating envelope. A detailed computer model was built in the MATLAB/Simulink environment to verify the HD-MMC algorithm with a closed loop control. The impact of the HD-MMC Set configuration and weighting factor on converter losses and *THD* were also evaluated using this model. Finally, the operating envelope of the modulation index, carrier frequency, Set configuration and power factor for the HD-MMC is investigated and potential improvements proposed.

The objectives of this chapter are therefore to:

- validate the HD-MMC in 3-phases with a closed loop control
- investigate the impact of the Set configuration on the generated losses and *THD*
- define the operating range of the HD-MMC
- maximise the operating range

To achieve these objectives, this chapter is organised as follows; the HD-MMC is evaluated in 3-phases with a closed loop control and the optimum configuration determined in Section 5.1. The limitations of the HD-MMC are then investigated in Section 5.2 and potential improvements to the algorithm discussed in Section 5.3. Finally, key outcomes of the chapter are given in Section 5.4.

5.1 Optimisation of the HD-MMC Parameters

The HD-MMC algorithm was shown to operate as expected in single-phase in Section 4.2, successfully maintaining stable SM capacitor voltages and generating the number of voltage levels specified. The *THD* was reduced compared to a C-MMC and was shown to be more efficient than using PWM. This section will investigate the HD-MMC algorithm in a 3-phase closed loop converter, through simulation in the MATLAB/Simulink environment. The models enable a more detailed investigation into the control parameters of the HD-MMC.

As discovered in Section 4.2, there are several factors that influence the performance of the HD-MMC, including the Set configuration and weighting factor. This section will further investigate the impact of these to determine their optimum settings. The switching frequency of the HD-MMC will therefore be compared to two C-MMC's, one with the same number of SMs as the HD-MMC and the other with the same number of voltage levels. This comparison will be performed over an operating frequency range of 50-2000 Hz. Finally, the comparative efficiency of the HD-MMC will be calculated with respect to the C-MMC over the same range.

5.1.1 Methodology and Simulation Set-up

This section outlines the MATLAB/Simulink model and methodology used to verify the proper operation of a 3-phase HD-MMC with outer control loops. An investigation into the impact of the weighting factor, Set configuration and operating frequency on converter performance is also conducted. To this end, six different 18 SM, HD-MMC Set configurations were simulated ([12 6 0], [9 9 0], [4 14 0], [6 6 6], [4 6 8], [4 4 10]). These were compared to three, C-MMC configurations with 18, 32 and 52 SMs ([18 0 0], [32 0 0] and [52 0 0] respectively). The [18 0 0] case is used as a control while the [32 0 0] and [52 0 0] cases create the same number of voltage levels as the most extreme two and three Set cases ([4 14 0] and [4 4 10] respectively). From these, the arm voltages and currents, Set and capacitor voltage imbalances and AC terminal frequency spectrums were calculated for three cases ([18 0 0], [4 14 0] and [32 0 0]) to verify the operation of the HD-MMC algorithm.

To investigate the impact of the weighting factors and Set configuration, each of the nine cases were run at 50 Hz with weighting factors between 0 – 20% of the nominal SM voltages. The capacitor voltage ripple, switching frequency and *THD* were calculated for each case and analysed to determine the optimum operating point for each. The [18 0 0], [4 14 0] and [32 0 0] cases were then selected and evaluated over an operating frequency range of 50 – 2000 Hz.

The switching frequency, conduction and switch losses were calculated for each case to determine the impact of operating frequency on the HD-MMC's performance.

To focus the analysis on the performance of the HD-MMC control algorithm, the MMC under test is connected to an ideal, 9.72 kV DC and 3.33 kV AC source and operated in inverter mode. The DC bus and AC grid are modelled using DC and 3-phase voltage sources respectively, as shown in Fig. 5.1 with the full circuit parameters summarised in Table 5.1. Each SM in the MMC consists of two ideal IGBT switches in parallel (s_p and s_s) with a SM capacitor (C_{mod}) as shown. Arm resistors (R_0) represent the lumped IGBT resistances and are included to ensure a realistic system dynamic performance; however, the converter losses were calculated separately using the manufacturer's data sheets as in Section 3.4. This ensures a more accurate loss calculation as IGBT resistance and switching energy are a function of arm current.

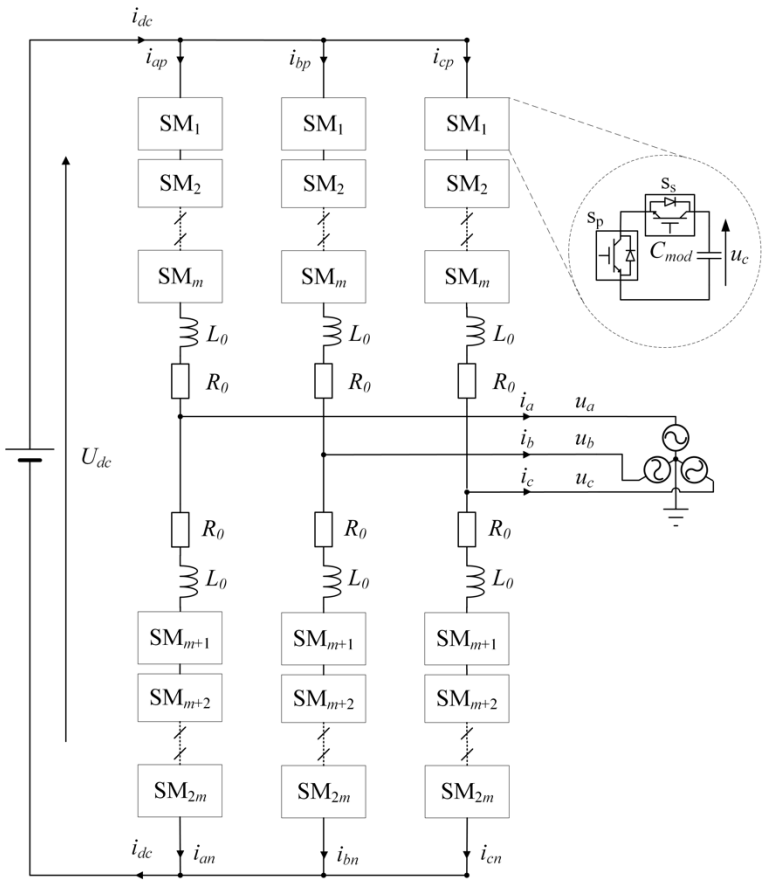


Fig. 5.1 The simulation set-up used to compare a 3-phase, 12 SM HD-MMC to a 12 SM and 32 SM C-MMC

The minimum arm inductance ($\check{L}_0$) and SM capacitance ($\check{C}_{mod}$) are calculated using (2.54) and (2.52) respectively. The C_{mod} is twice $\check{C}_{mod}$ as the converter was operated using NLM and the arm inductance three times that of $\check{L}_0$ to ensure it was far away from the second order harmonic resonance point. The arm capacitance (C_{arm}) and hence L_0 was held constant for each Set configuration to allow a fair comparison between the capacitor voltage ripples. The SM capacitance and arm inductances were recalculated from (2.52) and (2.54) respectively for each operating frequency and the grid inductance L_{grid} specified as a ratio of the arm inductance. The system dynamics therefore remain consistent over the frequency range.

Parameter	Symbol	Value			Unit
Set Configuration	$[\varsigma_1\ \varsigma_2\varsigma_3]$	[18 0 0]	[4 14 0]	[32 0 0]	
Number of voltage levels	n	19	33	33	
Set Voltages	$[u_{c1}, u_{c2}, u_{c3}]$	[0.56 0 0]	[0.312 0.625 0]	[0.312 0 0]	kV
DC Bus voltage	U_{dc}	9.72			kV
Real Power	P	10			MW
Reactive Power	Q	0.001			MVARs
Operating Frequency	f_0	50:2000			Hz
Weighting Factor	k_w	0:20			%
Arm inductance	L_0	(2.54)			mH
Arm equivalent resistance	R_0	4			mΩ/M
Arm capacitance	C_{arm}	(2.52)			mF
AC grid inductance	L_s	$2L_0$			mH
DC Bus Voltage	U_{dc}	10			kV
RMS Grid Voltage	U_{abc}	3.36			kV
Modulation Ratio	M	0.95			
Reference frequency	f_0	50			Hz
Sample per cycle	f_s	200			
IGBT Switch	Sw	Infineon-FF600R06ME3			
IGBT voltage rating	U_{ces}	0.6			kV
IGBT current rating	I_c	0.6			kA
Modulation Method		NLM			

Table 5.1 MMC and HD-MMC Simulation Specifications

The HD-MMC algorithm changes the voltage distribution between each SM compared to the equivalent C-MMC case. This creates a challenge to fairly compare the losses of the HD-MMC to a C-MMC, since any IGBT selected will favour one configuration over the other, influencing the results. If different IGBTs are permitted, the optimum switch may be selected for each configuration; however, the switch properties will no longer be consistent and a fair comparison still cannot be made.

Since the HD-MMC creates the additional voltage levels by creating partial voltage Sets, it effectively reduces the voltage rating of the converter. Therefore, the same switches will be used for each case and the potential of the highest voltage Set in the HD-MMC will be limited to the chosen switch's voltage rating. The primary application of the HD-MMC will be where the voltage range is restricted therefore, in the simulations, the nominal DC voltage will remain

constant, even for the [32 0 0] case. Instead the converter will be overrated, such that it contains more SMs than are required to withstand the voltage stress, as it would be in a real application if this option were chosen in place of the HD-MMC or C-MMC with PWM.

To calculate the converter losses, an Infineon FF600R06ME3 was selected for the converter IGBTs as it represents one of the lowest voltage, high power IGBTs on the market and hence a likely candidate for a MV MMC. From Table 5.1, the voltage and current rating of the IGBT are 0.6 kV and 0.6 kA giving the maximum DC voltage as 10.8 kV and with a 10% safety factor, the nominal DC voltage is 9.72 kV. The current to voltage and current to switching energy loss was calculated from the datasheet and used as in Section 3.4 to calculate the conduction and switching losses of each case.

5.1.2 Verification of the HD-MMC Algorithm in 3-phases

This section evaluates the operation of the HD-MMC control algorithm in the 3-phase converter model shown in Fig. 5.1 according to its two fundamental requirements as stated in Section 4.2.1. The first requirement is that the control algorithm generates the specified number of voltage levels which, in this case, is 33 according to (4.7) for the [4 14 0] example. The arm voltage and current of the converter are shown in Fig. 5.2a) and demonstrate that 33 levels have been generated. The arm current can be seen to have a large DC offset as expected; however, the second order harmonic has been successfully eliminated by the CCS as confirmed by the results of the FFT in Fig. 5.2b). The other even harmonics, particularly the 4th and 6th are still present as displayed in the FFT, although their contribution is small.

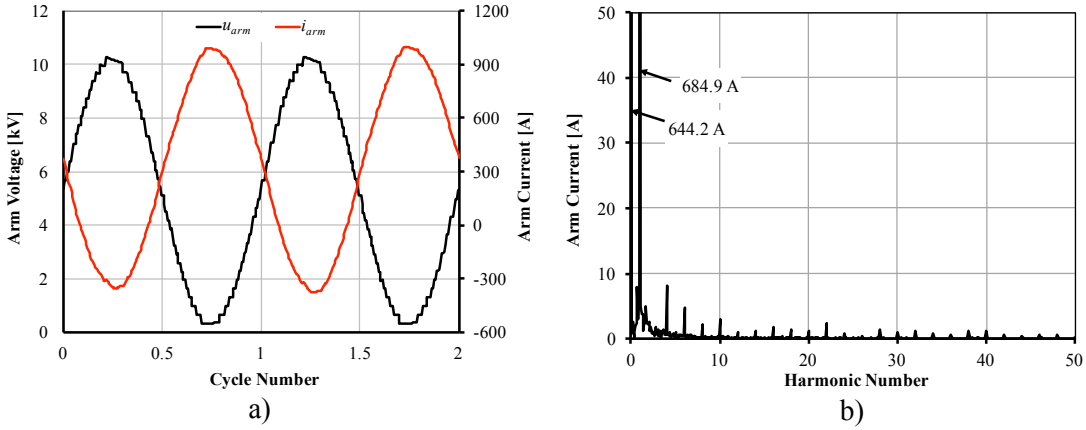


Fig. 5.2 The a) lower arm voltage and current waveforms over two cycles and b) the frequency spectrum of the arm current for the [4 14 0] configuration.

When the upper and lower arm voltages and currents are combined at the AC terminal, the DC offsets are eliminated (Fig. 5.3a)). The current and voltage waveforms can also be seen to be in phase and stable indicating that the outer power control is working properly. This is confirmed by examination of the real and reactive power output, shown in Fig. 5.3b), which is very stable deviating by around 0.2% from its nominal value.

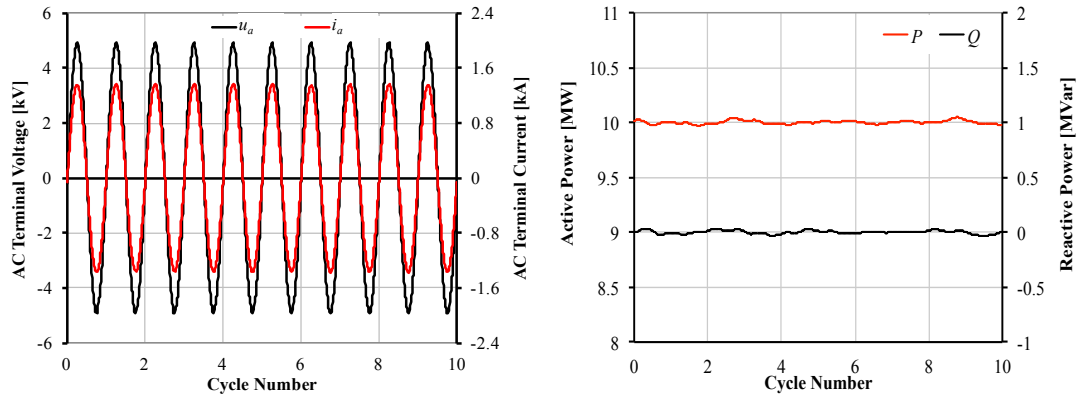


Fig. 5.3 The a) AC terminal voltage and current waveforms and b) output real and reactive power of the [4 14 0] configuration MMC

To be able to create stable and consistent voltage levels, the Set voltages must be maintained within tight tolerances. If they are permitted to stray too far, the upper and lower arm voltages will not be balanced. A potential difference will develop across the arm inductance which will drive a fundamental frequency circulating current. The converter losses and SM capacitor voltage ripple will increase impacting the capacitor life and control stability. From Fig. 5.4a) both Set voltages are stable and within 1% of their nominal value. For reference, the Set voltages of the [18 0 0] and [32 0 0] C-MMCs are also shown. The Set voltages are consistently around 0.5% below their apparent nominal value, apart from the first S_1 in the [4 14 0] configuration.

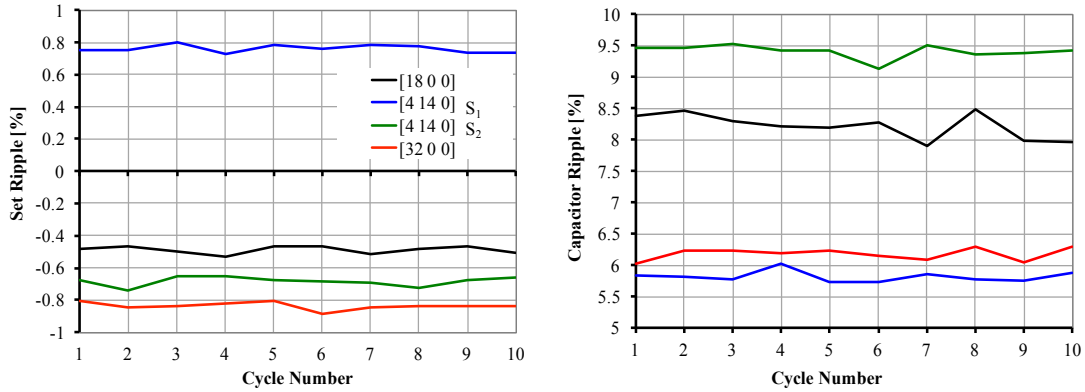


Fig. 5.4 The average voltage ripple over a cycle for the (a) Set and (b) SM capacitors for the [18 0 0], [4 14 0] and [32 0 0] configurations over 10 cycles.

In Fig. 5.4b) the maximum capacitor voltage imbalances over one cycle are seen to be consistent and within the desired 10%. Set 1 of [4 14 0] and [32 0 0] have the lowest voltage ripples because they have the highest switching frequencies. Comparing S_1 to S_2 of the [4 14 0] case, the maximum capacitor voltage ripple can be seen to be roughly 50% higher in S_2; however, the switching frequency is 25 kHz in S_1 compared to 18 kHz in S_2. With a higher switching frequency, the deviation between each SM voltage is minimised since when the voltage of one SM rises, it is quickly switched out in favour of a less charged SM. When the switching frequency is lower however, each SM is switched in for longer and so the converter power is no longer equally shared between the whole arm. Some SMs will therefore experience higher voltage ripples compared to others. This can be more clearly seen in Fig. 5.5 where the SM voltages are plotted over ten cycles.

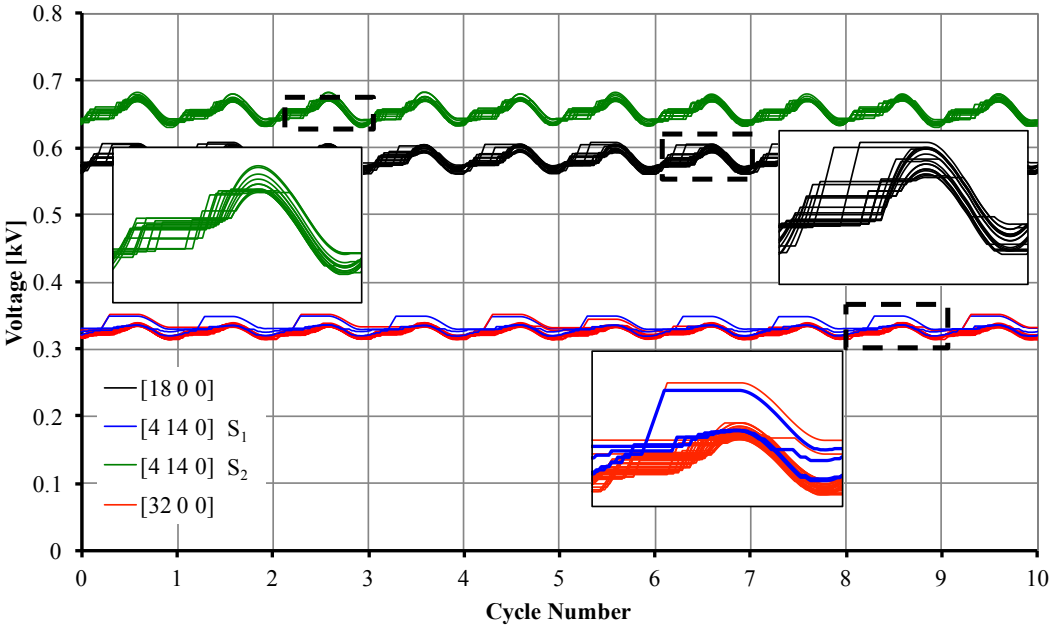


Fig. 5.5 SM capacitor voltages over 10 cycles for each Set of the [18 0 0], [4 14 0] and [32 0 0] MMC configurations.

The switching frequency of the lowest voltage Set will always be greater than the higher voltage Sets especially for the Set voltage ratio used in this example (U_r = [1 2 4]). This is because the creation of any odd voltage level requires the switching of at least one SM from the lowest voltage Set.

5.1.3 Investigation of the weighting factor and Set configuration

This section contains a detailed investigation into the impact that the SM balancing weighting factor and the Set configuration have on the HD-MMC's performance. Simulations of the nine configurations mentioned in Section 5.1.1 were run with weighting factors ranging from 0 – 20% at an operating frequency of 50 Hz. The maximum SM voltage ripples of each Set, switching frequencies and AC terminal *THD*s were calculated and the results analysed in turn below.

The switching frequency and SM voltage ripples are plotted against the weighting factor for the C-MMC cases in Fig. 5.6a) and the two Set and three Set HD-MMC cases in Fig. 5.6b) and Fig. 5.6c) respectively. In all the cases, the weighting factor has a very large initial impact on the switching frequency, greatly reducing it between 0 and 2%. Above 2%, this quickly tapers off and it has little further impact on switching frequency in any configuration. The weighting factor biases SMs that are already switched in by a percentage of their nominal

value so that they will move to the top or bottom of the sorting list. If the converter is designed properly, the SM voltages should not change by much more than 10% over the whole cycle. Therefore, the spread of the SM voltages at each time step should be relatively tight as shown in Fig. 5.5. As a result, only a very small bias is required to influence the location of the SM within the sorted stack and hence whether it is selected to remain switched in or not.

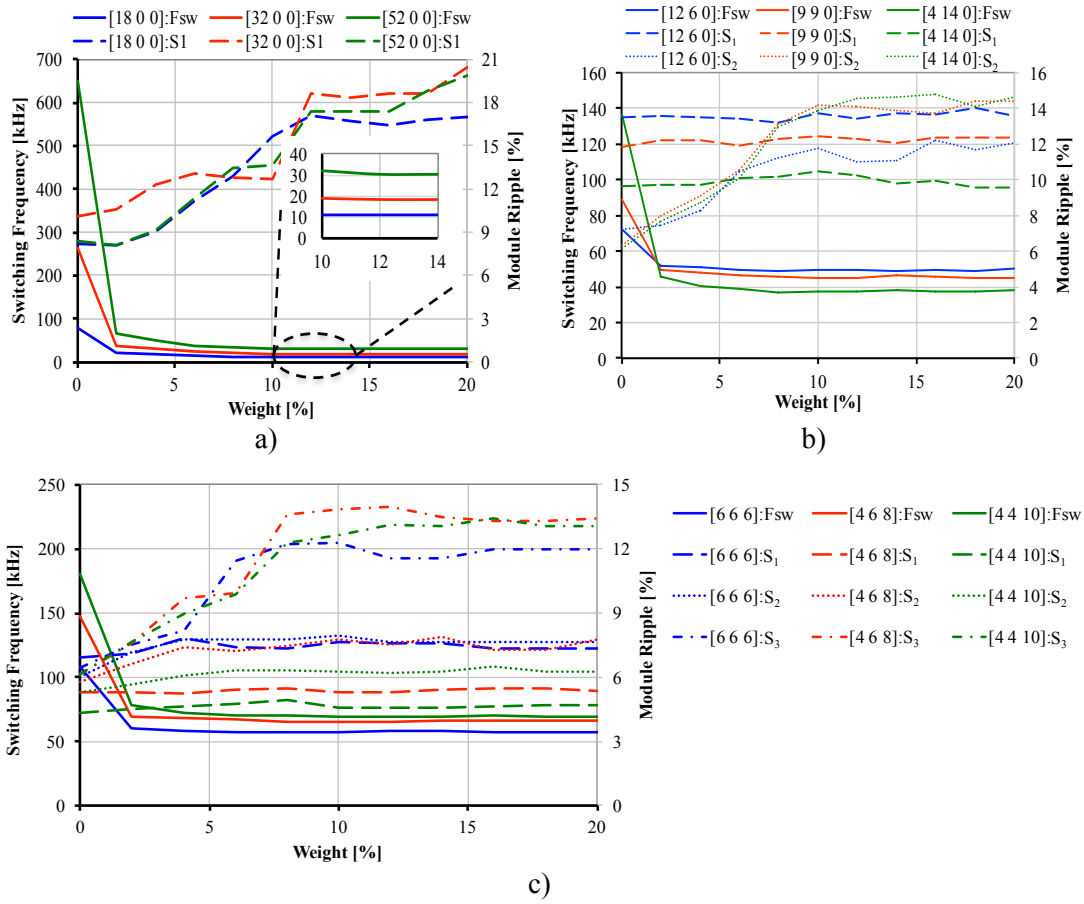


Fig. 5.6 The switching frequency (Fsw) and maximum SM voltage ripple for each Set are plotted against the weighting parameter for the; a) C-MMC b) 2S HD-MMC; c) 3S HD-MMC configurations.

The largest initial reductions in switching frequency are observed in the C-MMC cases with the [52 0 0] showing the greatest impact (Fig. 5.7). This is because as the number of SMs in the C-MMC increases, the maximum number of SMs that the SM balancing algorithm can change at any switching point (SM_{max}) increases. For example, in the 18 SM C-MMC, a maximum of nine SMs can be changed at any one time, in the 52 SM C-MMC however, 26 could be swapped. As the weighting factor increases, SM_{max} will approach 1.

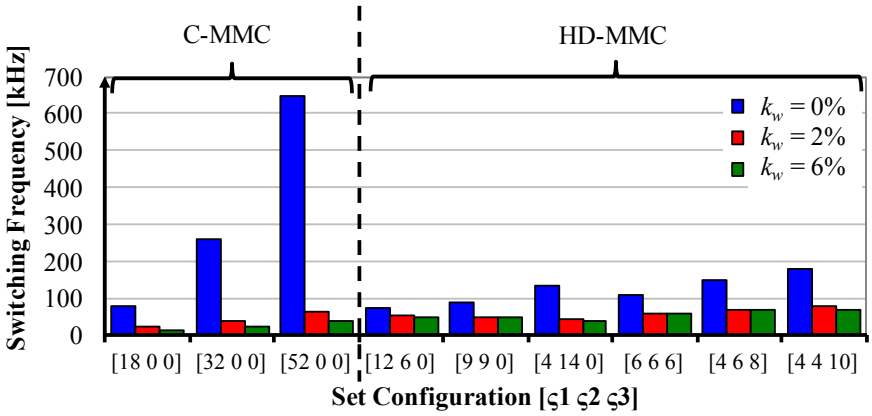


Fig. 5.7 The switching frequency plotted as a function of the MMC configuration for three weighting factors: 0, 2 and 6%.

In the HD-MMC cases, the greatest reductions occur in the configurations with the most SMs in the highest voltage Set; however, the configurations that generate the highest number of voltage levels do not always have the highest switching frequencies. For example, the [4 14 0] case has the lowest switching frequency of all the two Set HD-MMC cases. To see why this occurs, the average switching frequency of SMs within each Set of the two Set HD-MMC cases are plotted against the weighting factor in Fig. 5.8. There are 3 things of interest in Fig. 5.8:

1. The reduction in SM switching frequency in each Set, as the weighting factor is increased, is proportional to the number of SMs in that Set.
2. At a weighting factor of 0 %, the switching frequency increases for all Sets with the number of voltage levels created, consistent with the C-MMC cases.
3. At weighting factors of more than 2 %, the switching frequency of SMs in S_2 and S_1 decreases as the number of SMs in it increases, the opposite of the C-MMC cases.

The first two points are to be expected for the same reasons noted for the C-MMC cases; however, the third observation requires additional explanation. The root cause of this peculiarity can be traced back to the HD-MMC algorithm. While it is likely present in all the HD-MMC cases, it has a smaller effect on the switching frequency than the SM balancing controller. To reveal its impact, the weighting factor must be raised high enough to mitigate the additional switching events normally created by the SM balancing controller.

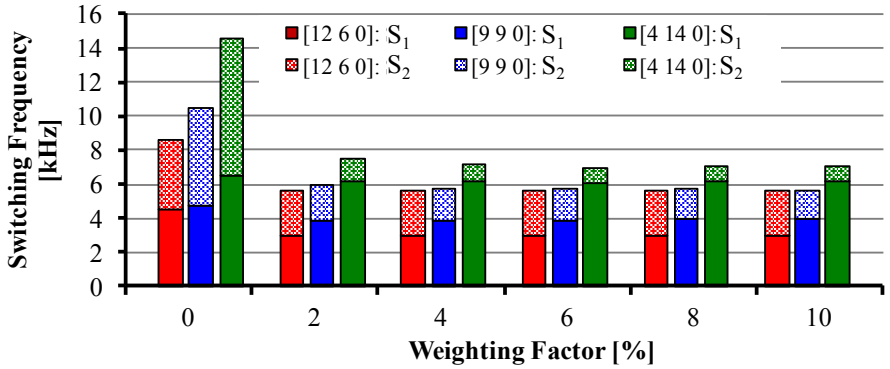


Fig. 5.8 The average switching frequency of each SM within each Set of the 2S HD-MMC cases at weighting factors between 0 and 10 %

If a Set combination table is created for each case, such as that shown in Table 4.2, it is possible to calculate SM_{max} between different voltage levels. These have been calculated for the three, two Set HD-MMC cases, as shown in Table 5.2. The maximum change has been selected because the Set controller will only consider a maximum of two Set combinations in the two Set HD-MMC; the one with the maximum, or minimum number of SMs switched in for the Set with the largest deviation.

		[12 6 0]	[9 9 0]	[4 14 0]
Max change in SMs inserted per level (SM_{max})	[S_1 S_2]	[11.0 6.00]	[9.00 5.00]	[3.00 2.00]
Mean change in SMs inserted per level (SM_{mean})	[S_1 S_2]	[6.00 3.00]	[6.04 3.00]	[2.75 1.75]
Normalized change in SMs inserted per level (SM_{nom})	[S_1 S_2]	[0.50 0.50]	[0.67 0.33]	[0.69 0.13]

Table 5.2 Two Set HD-MMC calculation table

Table 5.2 shows that SM_{maxy} for the y^{th} Set depends on ς_1 to ς_g according to:

$$SM_{max1} = min\left\{\varsigma_1 + \frac{1}{2}((-1)^{\varsigma_1+1} - 1),\ U_{r2}\varsigma_2\right\} \tag{5.1}$$

$$SM_{max2} = min\left\{\frac{U_{r1}}{U_{r2}}(\varsigma_1 + \frac{1}{2}((-1)^{\varsigma_1} - 1)),\ \varsigma_2\right\} \tag{5.2}$$

where SM_{max1} is the SM_{max} of S_1 and SM_{max2} is the SM_{max} of S_2. As a result, in the [12 6 0] case, $SM_{max2} = 6$ while in the [4 14 0] case $SM_{max2} = 2$, even though ς_2 more than twice the value in the [4 14 0] case. This only tells part of the story however, since from Fig. 5.9, it can be seen that SM_{max} is only possible for a proportion of the number of switching voltage levels.

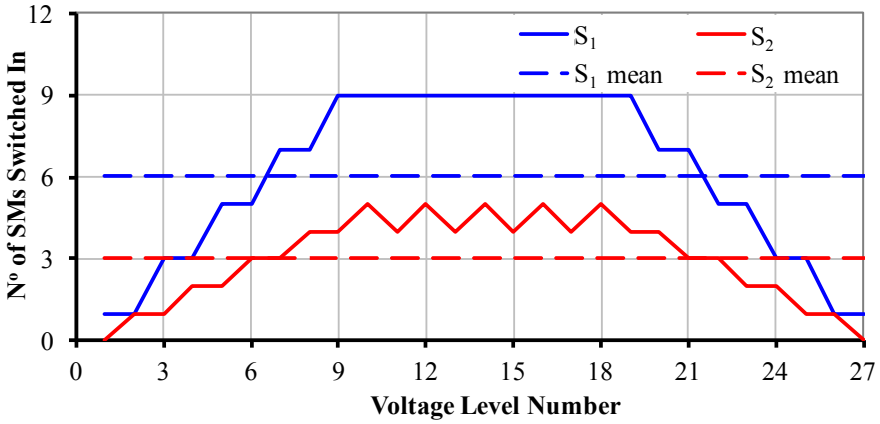


Fig. 5.9 Maximum change in the number of SMs that can be selected between two voltage levels (SM_{max}) plotted against the voltage level number for the [9 9 0] case

By taking the mean of SM_{max} for each voltage level i_n, the average SM_{max} can be calculated for each Set (SM_{mean})

$$SM_{mean} = \frac{1}{n}\sum_{i_n=1}^{n} SM_{max_{i_n}} \tag{5.3}$$

Then, if this mean is normalised with respect to the number of SMs present in each Set (SM_{nom}) as shown in Table 5.2, the results will be in the same format as the switching frequencies displayed in Fig. 5.8.

$$SM_{nom\_y} = \frac{SM_{mean\_y}}{\varsigma_y} \tag{5.4}$$

Now it can be seen that the reason S_2 in [4 14 0] has the lowest number of switching events despite having the most SMs in it, is because it has the lowest per unit SM_{max}. This has significant design implications when considering the Set configuration, as a high number of voltage levels can be created while still maintaining a reasonable switching frequency.

While there is little change in the switching frequency above the 2% weighting factor, the capacitor voltage ripple of the highest voltage Set continues to increase (Fig. 5.6). While most of the SMs are unaffected by the weighting factor above 2 %, the SMs that have the highest duty for a cycle or experience the largest magnitude arm current, will still be affected. These may not create a significant difference to the total switching frequency however, they do impact on the maximum SM voltage ripple. This has a significant effect on the life of metallised film capacitors such as those commonly used as SM capacitors [158] and as such should not be ignored. This voltage ripple is also reflected in the AC terminal voltage with an increase in *THD* (Fig. 5.10). The lower voltage Sets are largely excluded from these effects

(Fig. 5.6) as they have a naturally higher switching frequency. However, the weighting factor should still be chosen to be as low as possible, since the highest voltage Set is still heavily affected.

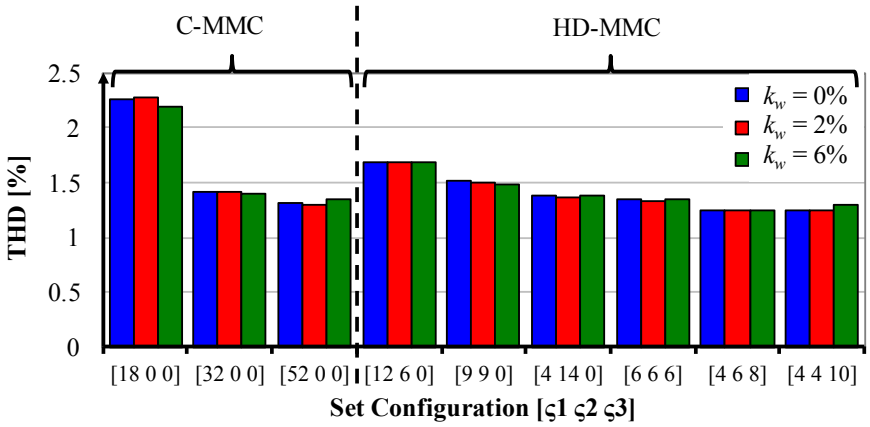


Fig. 5.10 The Total Harmonic Distortion plotted as a function of the MMC configuration for three weighting factors: 0, 2 and 6%.

Through examination of Fig. 5.10, the *THD* calculated for the C-MMC cases can be seen to be equivalent to the HD-MMC cases. Furthermore, the reduction in *THD* with increasing voltage levels clearly follows the law of diminishing returns; however, the switching frequency continues to rise. In this case, there does not appear to be much advantage in using three Sets to boost the number of voltage levels created and [4 14 0] is likely to be the optimal configuration. This may change however, if there are fewer SMs in the arm and the starting *THD* is larger.

5.1.4 Power loss analysis of the HD-MMC

The primary goal of developing the HD-MMC was to create a more efficient method to reduce the *THD* of MMCs in the MV range. This could previously only be accomplished by either introducing PWM or by increasing the number of series connected SMs per arm, at the expense of overrating the converter. Section 4.2 and Section 5.1 explored the relationship between the switching frequency and *THD* at 50 Hz; however, it is known from Section 3.5, that as the converter's operating frequency increases, the switching frequency becomes more influential. As the HD-MMC algorithm increases the switching frequency of SMs in lower Sets, it is important to verify that the switching frequency of the HD-MMC has a similar linear relationship to the operating frequency as in the C-MMC cases. Furthermore, up to this point, the relative efficiency of the HD-MMC to the C-MMC has been inferred from the switching

frequency. In this section, an example 10 kV, 10 MVA converter is used to compare the relative conduction and switching losses of three converter configurations, the [18 0 0], [32 0 0] and the [4 14 0]. As explained in Section 5.1.1, the DC bus voltage of the HD-MMC case is reduced to allow the same IGBT switches to be used for each comparison.

To check the behaviour of the HD-MMC's switching frequency with respect to the operating frequency, two configurations were selected from the C-MMC, two Set HD-MMC and three Set HD-MMC. Their switching frequencies were plotted against the operating frequency in Fig. 5.11 with a weighting factor of 2% as this was found to be the optimum in Section 5.1.3.

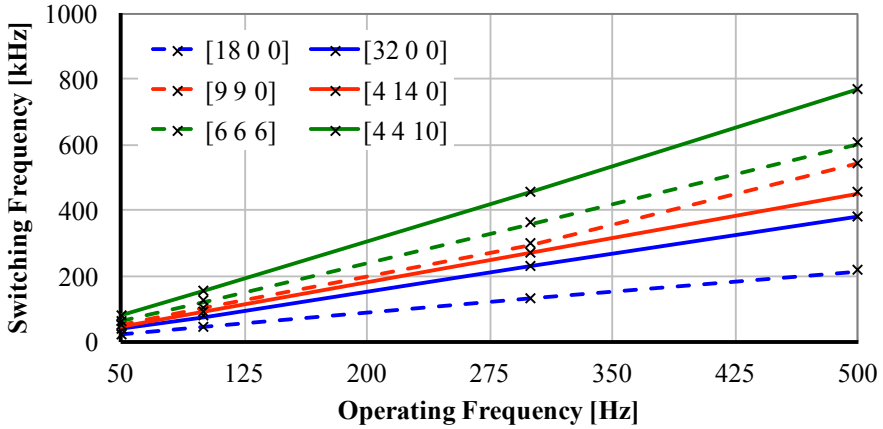


Fig. 5.11 The switching frequency plotted against the operating frequency for a selection of HD-MMC and C-MMC configurations at a 2% weighting factor.

As it can be seen, a linear relationship exists for each case although the HD-MMC configurations have a greater gradient than those of the C-MMC. As a result, there will exist a frequency when it becomes more efficient to use the C-MMC with additional voltage levels rather than the HD-MMC. Comparing the [32 0 0] and [4 14 0] cases however, this is likely to be at a very high operating frequency since the difference in gradient is very small. Indeed, when the full losses of the converter are calculated for these two cases, the [4 14 0] configuration is found to be more efficient even at 2 kHz (Fig. 5.12). The three Set HD-MMC cases have the highest switching frequency for only a marginal improvement in *THD*. This case therefore does not warrant the additional switching loss and it is not investigated further.

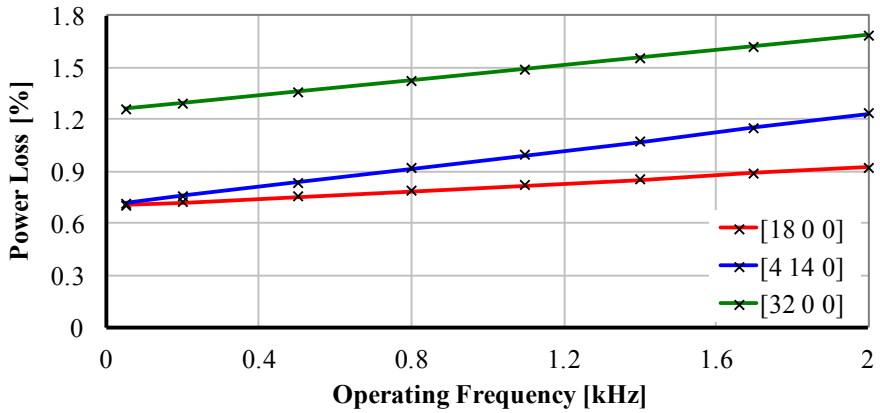


Fig. 5.12 Total converter loss for the [18 0 0], [32 0 0] and [4 14 0] cases from 50 to 2000 Hz

In Fig. 5.13, the operating losses are broken down into the switching and conduction losses for the [18 0 0], [32 0 0] and [4 14 0] configurations over a range of operating frequencies. As it can be seen, the conduction losses remain consistent for each configuration over the whole frequency range; however, the switching losses increase. The [4 14 0] configuration sees the largest rise in switching losses as predicted by Fig. 5.12 however, it remains more efficient than the equivalent C-MMC case ([32 0 0]).

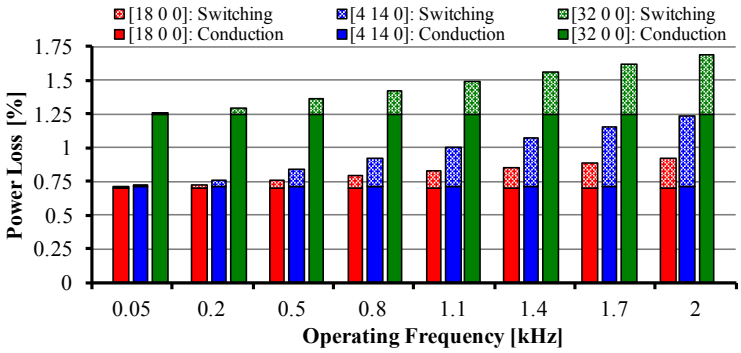


Fig. 5.13 Breakdown power loss of the [18 0 0], [32 0 0] and [4 14 0] configurations over the MF range

While the conduction losses are marginally higher (0.84%) in the [4 14 0] case, compared to [18 0 0] case this is significantly lower than expected. The DC bus voltage of the [4 14 0] case is 11% lower than the [18 0 0] case which should lead to 25% increase in power loss. However, the arm current harmonics are also reduced in the [4 14 0] case which counteracts some of the increase in current magnitude. On average the arm current *THD* is 50% lower in the [4 14 0] case compared to the [18 0 0] case.

5.2 Operational Range of the HD-MMC's Set Control

Before the HD-MMC algorithm can be implemented, it is important to define its operational range, in terms of not only the hardware configuration but also the control parameters. Variables such as the carrier frequency and modulation strategy are known from Section 2.1.2 to greatly influence the SM voltage ripple and AC terminal *THD*. Since the magnitude of the Set voltage ripple is determined by SM voltages within it, this may have an impact on the HD-MMC's stability. Another important control parameter is the power factor as this determines the angle between the arm voltage and current; hence, it determines how many SMs and under which configuration they experience the peak current stress. Since the HD-MMC works by repurposing redundant states, some power factors could fall into sensitive zones where the HD-MMC algorithm is unable to maintain Set stability. The effect of the switching frequency and power factor on the HD-MMC algorithm's ability to maintain control of the Set voltages is therefore investigated in Section 5.2.1 and any limitations defined.

From Section 5.1 it is known to be beneficial to minimise the number of SMs in the lowest voltage Set. This increases the number of voltage levels that can be generated and reduces the reduction of the DC voltage range created by inserting partial voltage SMs. Furthermore, the HD-MMC is of particular interest for power converters operating in the MV and LV range, where the number of SMs in each arm are limited. This also means that each Set will contain fewer SMs. In both cases the number of redundant states is reduced, which will subject the HD-MMC algorithm to additional stress. Since the algorithm relies on these redundant states to maintain the Set voltages, there will be a minimum number of SMs per Set, beyond which, the Set voltages will begin to diverge. The effects of this started to appear in cases 13 – 15 presented in Section 4.2 and are further investigated in Section 5.2.2.

5.2.1 The Effect of the Control Parameters on Set voltage stability

This section investigates the HD-MMC algorithm's ability to maintain the Set voltages at power factors ranging from 0 – 1 and different modulation strategies. NLM, as well as PSC PWM with carrier frequencies ranging from 3– 32 times the operational frequency, which was kept at 50 Hz for all cases. As the first potential limitations of the HD-MMC were observed using [3 15] configuration (cases 13 – 15) of Section 4.2, a [3 3] converter configuration was used here. While different from the [3 15] case, it has the same minimum number of SMs in the first Set and fewer in the second so will still tax the HD-MMC algorithm.

The operational range of the control Set points of the converter should be tested using the full control to replicate actual use as the additional harmonics generated by the CCSC influences the SM voltage stability. In Fig. 4.9 the outer power control loops are shown to generate a reference value e_j that determines the modulation index and control the real and reactive power flow in the converter. In a MMC, the modulation index not only determines a switch's duty ratio but also the maximum number of SMs that are inserted in a cycle. In the HD-MMC this will also affect the Set combinations that are used in each cycle and hence have an impact on the HD-MMC algorithm's ability to balance the Set voltages. The carrier frequency and modulation index will therefore be tested for modulation indexes 0.5 – 1. The converter however, is designed to operate at its optimum modulation index to maximise efficiency so it is unlikely that it would operate below 0.5.

The modulation index is normally used to affect the desired change in the converter's reactive power output and hence power factor. To test the power factor range at each modulation index then, the connection between the power factor and modulation index must be broken. This is accomplished here through an additional control loop (Fig. 5.14) that increases the AC grid voltage to maintain a constant modulation index. The algorithm controls the AC terminal voltage so that the magnitude of the converter current is unaffected. It is acknowledged that this could create a control instability; however, it represents the best option available. While the reactive power control could be altered to directly influence the AC grid voltage, it is preferred to leave the control unaltered. A constant load could also be used in place of the AC grid; however, this would mitigate the power control altogether.

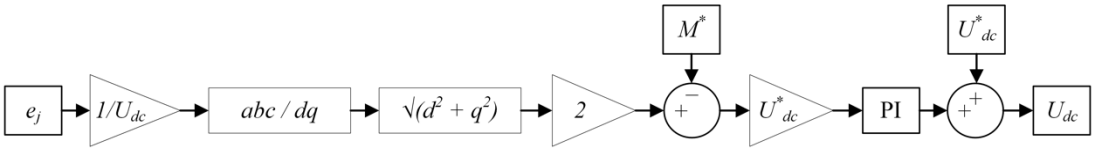


Fig. 5.14 Control loop used to control the DC voltage bus to achieve the desired modulation index in the PWM control

The [3 3] configuration was simulated with an operating frequency of 50 Hz and carrier at 250 Hz ($5f_0$) at power factors ranging from 0 – 1 and modulation indexes of 0.5 – 1. From the surface plot in Fig. 5.15, the Set voltage deviation remains low (< 2%) for most operating conditions. At high power factors and modulation indexes between 0.85 – 0.95 however, the average Set voltage deviation increases significantly to > 7 %.

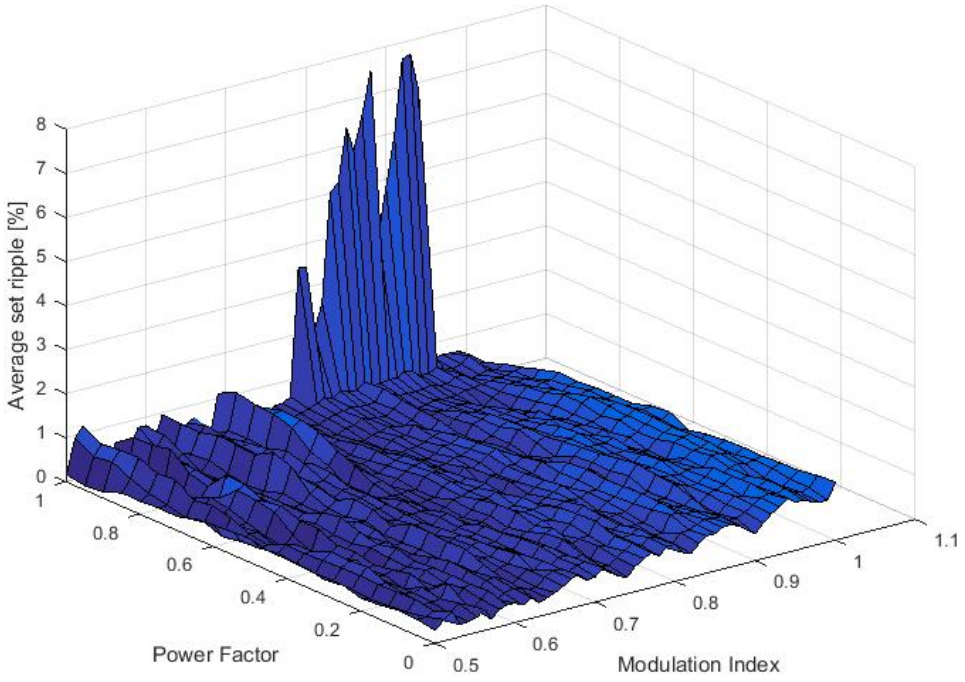


Fig. 5.15 The average Set voltage ripple of all four Sets in the branch plotted against *pf* and *M*

This can be more clearly seen in Fig. 5.16 where the Set deviation of each Set in the branch at unity power factor and a carrier wave frequency (f_{cr}) of 250 Hz is plotted against the modulation index. The individual Set voltage deviations here are much higher than the average values, particularly in the lower voltage Sets where deviation exceeds 20% at its peak. The Set controller clearly cannot properly manage the Set voltages in this region leading to unstable converter behaviour. In previous cases, the HD-MMC was operated with a $M > 0.95$ to maximise efficiency, as a result, this effect was not evident.

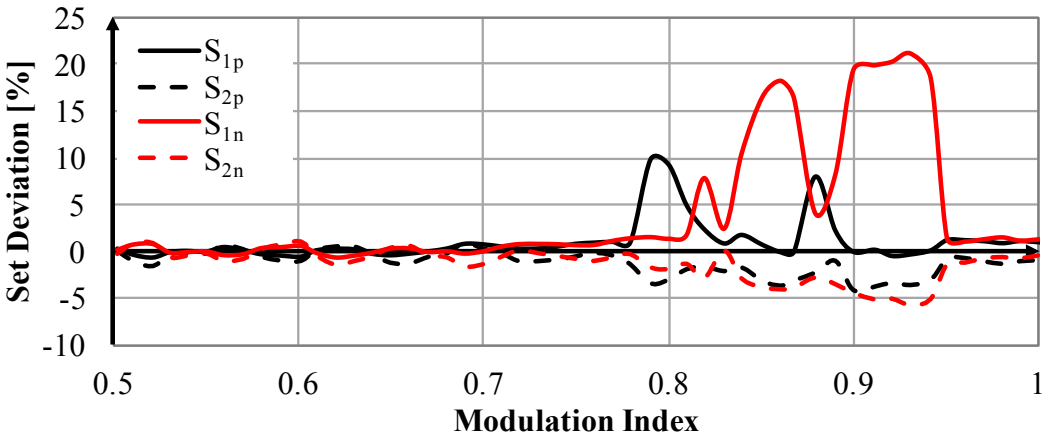


Fig. 5.16 The deviations of the Set voltages from their nominal values are plotted against the *M* at $pf = 1$

The HD-MMC control algorithm assumes that the Set voltages remain within a tight tolerance of their nominal values; when this ceases to be valid, the step magnitudes become uneven and the arm voltages unequal, as shown in Fig. 5.17. This drives an uncontrolled fundamental harmonic circulating current within the converter, thereby reducing efficiency and potentially overrating the components. This also increases the *THD* at the AC terminal, negating some of the benefits of the HD-MMC as demonstrated in cases 13 – 15 in Section 4.2.3.

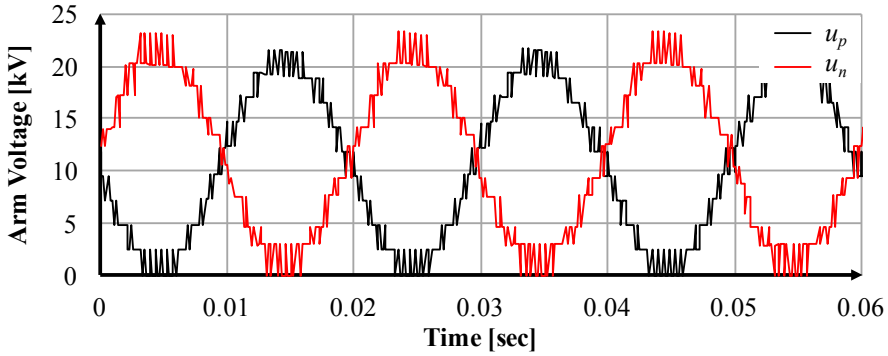


Fig. 5.17 The upper and lower arm voltages of phase a

The Set voltages are the sum of the SMs contained within them and as such, are directly influenced by the stability of the SM voltages themselves. When a SM is inserted, it will begin to charge or discharge according to:

$$u_c = \frac{1}{C_{mod}} \int i_{arm} dt \tag{5.5}$$

The arm current magnitude and length of time that the SM is inserted determine how far the inserted SMs deviate from those that are switched out. The SM capacitance is calculated based

on the arm current as in Section 2.1.3, so the main variable is the continuous time duration that the SM is inserted for. If the continuous period that the SM is switched in for is too long, the SM's voltage deviates significantly from the rest of the Set. In the C-MMC the SM voltage deviation is managed by increasing the carrier frequency and so it stands to reason that this would also affect the Set voltage.

The carrier frequency was therefore increased from 1 (NLM) to 32 times the converter operational frequency at modulation ratios 0.5 – 1 with the power factor Set to 1. A unity power factor was chosen since as can be seen from Fig. 5.15, the HD-MMC algorithm only appears to struggle around this value. When the results are plotted in the surface plot in Fig. 5.18 it can be seen that there are no discernible carrier frequency limitations. The Set voltage ripple is poor for *M* between 0.75 – 1 for both NLM and PWM with carrier waves across the spectrum (150 – 1150 Hz).

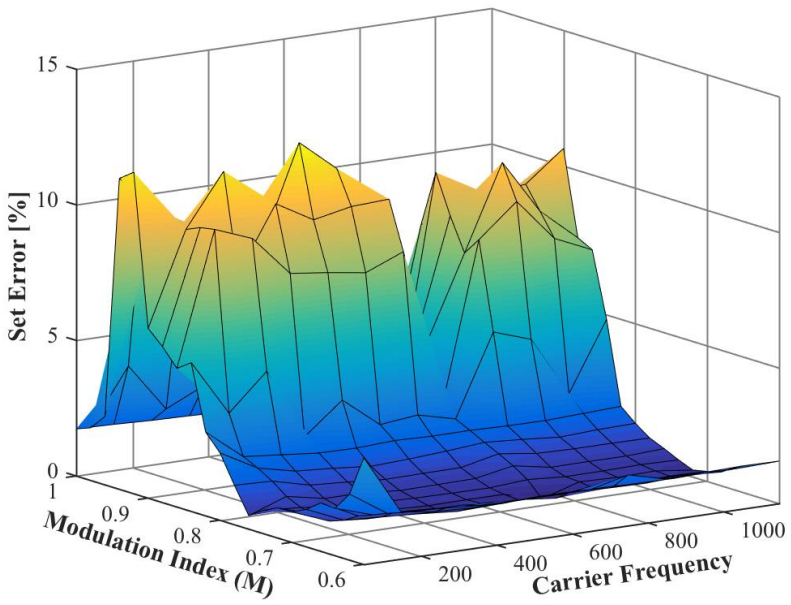


Fig. 5.18 The average Set voltage ripple at unity power factor plotted against the M and f_{cr}

When *M* is increased slightly above 1, the Set voltage ripple rapidly decreases again below 1%. Combining the results presented in Fig. 5.15 and Fig. 5.18 the HD-MMC algorithm struggles when it must operate close to a unity power factor between modulation indexes 0.75 – 1 when $\varsigma_1 = 3$. This is problematic as these regions coincide the areas of highest converter efficiency and hence where the converter is normally designed to operate. The STATCOM is

a notable exception to this as it is used for reactive power compensation but would present a limited market for the HD-MMC algorithm.

5.2.2 The effect of converter configuration on Set voltage stability

The Set voltage stability was found to be unaffected by the carrier frequency in Section 5.2.1 but suffer limitations at unity power factor between modulation indexes 0.75 – 1 in the [3 3] configuration. The Set configuration directly influences the number and position of the redundant states (Fig. 5.19) which are used by the HD-MMC control algorithm to balance the voltages. The Set configuration may therefore have a significant impact on the control stability and will be explored in detail in this section.

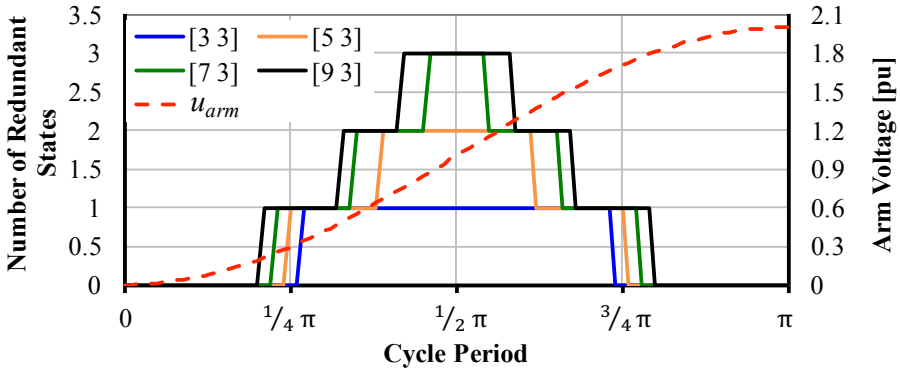


Fig. 5.19 The number of redundant states available at each point in half a cycle of a cosine wave for 5 Set configurations [3 3], [5 3], [7 3], [9 3]

This is done for ς_2 increasing from 2 – 5 in Fig. 5.20a) – Fig. 5.20d) respectively to demonstrate the impact of the second Set. For each case, the number of SMs in the first Set has a significant impact on the Set error, with the error reducing from > 30% for ς_1 = 2 to < 1% for ς_1 = 5.

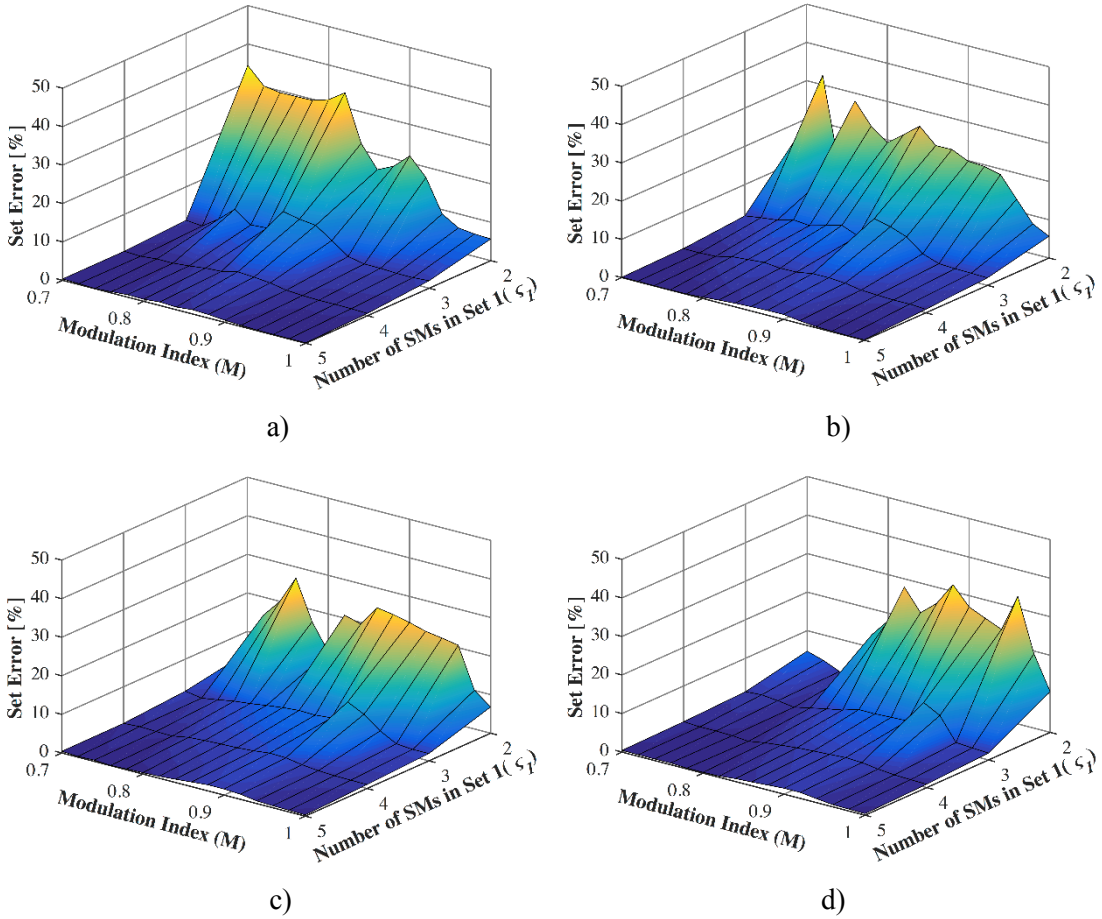


Fig. 5.20 The Set error as a function of ς_1 and M for a) $\varsigma_2 = 2$, b) $\varsigma_2 = 3$, c) $\varsigma_2 = 4$ and d) $\varsigma_2 = 5$

The Set error significantly improves over much of the modulation index range once $\varsigma_1 = 3$ but there is little improvement between $\varsigma_1 = 4$ and $\varsigma_1 = 5$ or through increasing the number of SMs in S_2.

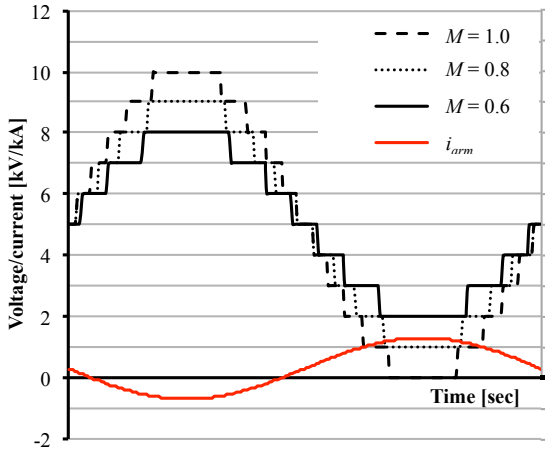
When $\varsigma_1 = 3$ the Set error is marginal for much of the modulation index range; however, there are spikes at localised modulation indexes. The range over which the spikes occur and the position on the modulation index axis increases with the number of SMs in S_2. To explain this, it is useful to translate the modulation index into the number of SMs omitted in each cycle (SM_{omit}) which is calculated from (5.6) below.

$$SM_{omit} = \big((n-1) - M(n-1)\big) \tag{5.6}$$

$$SM_{min} = 0.5 \cdot SM_{omit} \tag{5.7}$$

$$SM_{max} = n - 0.5 \cdot SM_{omit} \tag{5.8}$$

The omitted SMs have an equal effect on the peak and minimum points of u_{arm} (Fig. 5.21) such that the minimum number of SMs inserted (SM_{min}) and maximum number of SMs inserted (SM_{max}) are given by (5.7) – (5.8) respectively.



Level	S_1	S_2
10	4	3
9	3	3
8	2	3
7	1 or 3	3 or 2
6	0 or 2 or 4	3 or 2 or 1
5	1 or 3	2 or 1
4	0 or 2 or 4	2 or 1 or 0
3	1 or 3	1 or 0
2	0 or 2	1 or 0
1	1	0
0	0	0

Fig. 5.21 Arm voltages for different M and table showing SMs required to create the corresponding voltage level. Where there are multiple options available i.e. for 6L, the SMs required for each option is shown in the square brackets.

SM_{min} is plotted the Set error in Fig. 5.22a) – d) for 2 – 4 SMs in S_2 and 3, 4 and 5 SMs in S_1. The Set error begins to spike as the number of SMs omitted approaches 0.5 and remains elevated until the number of SMs omitted approaches 1.5. Here, a fraction of an SM is omitted if the SM's duty is reduced to better approximate the AC reference waveform. That is to say, if the AC reference waveform does not result in an integer number of SMs inserted, the NLM control will reduce the amount of time each SM is inserted, such that the average voltage approximates the reference AC waveform.

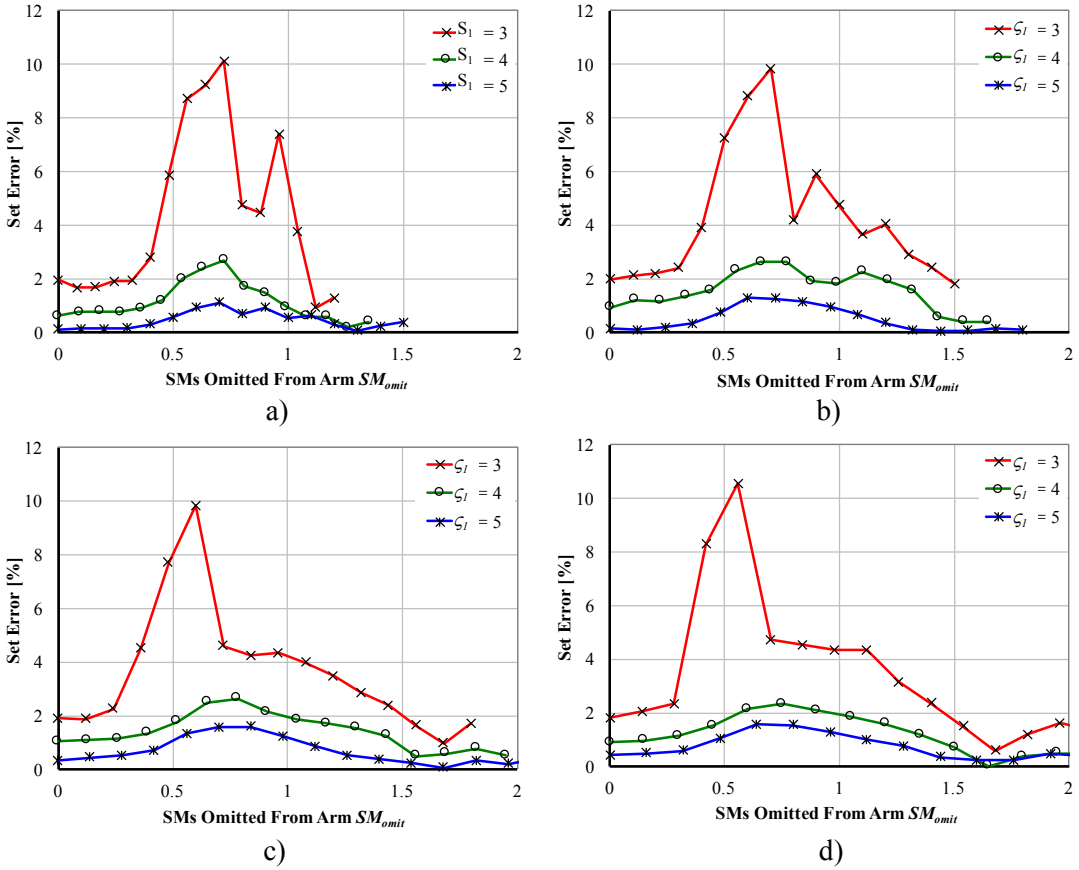


Fig. 5.22 Set voltage error vs. the number of SMs omitted in each cycle where $\varsigma_1 = 3$, 4 and 5 for a) $\varsigma_2 = 2$, b) $\varsigma_2 = 3$, c) $\varsigma_2 = 4$ and d) $\varsigma_2 = 5$

The size of the spike reduces for all cases as the number of SMs in S_1 increases however, its position remains constant. Its position changes in Fig. 5.20a) – Fig. 5.20d) because as the number of voltage levels created increases from 5 to 16, for the same reduction in *M*, the number of SMs omitted increases. Therefore, the spike moves to higher *M* values as the number of SMs, and hence levels increases. The most significant contribution to the Set error comes from S_1 (Fig. 5.23) which is consistently overcharged in each case. The cases run in this section were for a 10 MW (export) converter at unity power factor and as such the arm voltages and currents are 180° out of phase (Fig. 5.24).

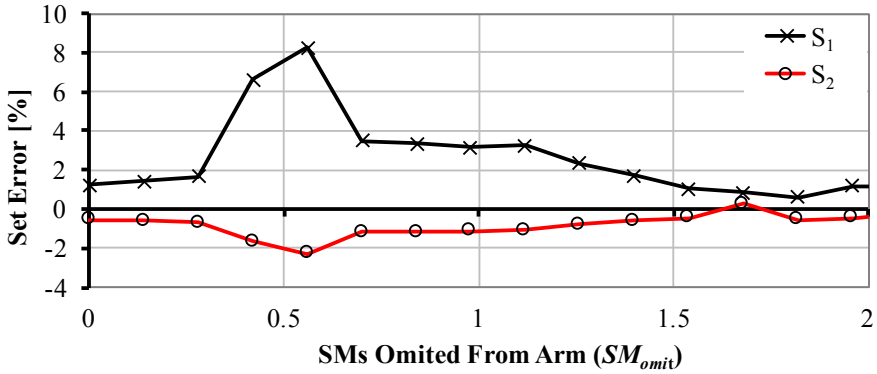


Fig. 5.23 Set voltage error for S_1 and S_2 in a [3 5] converter configuration for an increasing number of SMs omitted.

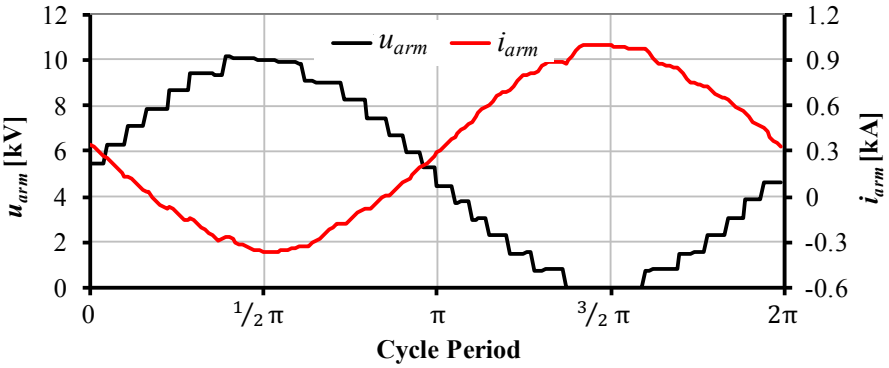


Fig. 5.24 Arm voltage and current for the [3 5] converter configuration exporting 10 MW at $pf = 1$

Therefore, the peak current occurs when SM_{min} is inserted. When $M = 1$, no SMs are inserted at this point and as such all Sets are equally unaffected. As the modulation index reduces however, SM_{min} increases. When the modulation index is low enough, $SM_{min} = 1$ and $SM_{\max} = n - 1$ the i.e. when the arm current is at the minimum and maximum points (Fig. 5.21). From Fig. 5.21, if $M = 0.8$, 1 SM from S_1 must support the peak current in the trough of the arm voltage waveform. In the table next to Fig. 5.21, it can be seen that there is only one Set combination option available (1 SM in S_1 and 0 SMs in S_2) and hence there is no Set redundancy. To compound the issue, this is repeated in reverse at the top of each waveform where minimum arm current occurs and SM_{max} SMs are inserted. When a SM is omitted from the lowest voltage point, it is also omitted from the highest point, therefore, S_1 is solely exposed to the highest current and has the lowest proportion of its SMs inserted at the minimum current. Taking the $M = 0.8$ case from Fig. 5.22 as an example, it is demonstrated in (5.9) – (5.11) that S_2 will discharge 50% more at the top of the cycle (depending on the current direction) since the current through the SMs in each Set is the same.

$$U_{mod} = \frac{1}{C_{mod}} \int i_{arm} dt \tag{5.9}$$

$$\Delta U_{mod} = \frac{1}{C_{mod}} \int_{T1}^{T2} I_{arm}(t) \cdot dt \tag{5.10}$$

$$\Delta S_1 = 2\Delta U_{mod};\ \Delta S_2 = 3\Delta U_{mod} \tag{5.11}$$

From Fig. 5.19, the highest number of redundant states occurs when the current is at a minimum and as such is not sufficient to redistribute the voltage imbalance. When the modulation index decreases further and two SMs are omitted, there is Set redundancy at the maximum and minimum current positions and so the imbalance does not occur.

In Fig. 5.25, the Set error is plotted as a function of the modulation index and number of SMs in S_1 for a converter with 2 to 5 SMs in S_2 and 2 SMs in S_3 and is repeated for 3, 4 and 5 SMs in S_3 in Fig. 5.26 to Fig. 5.28.

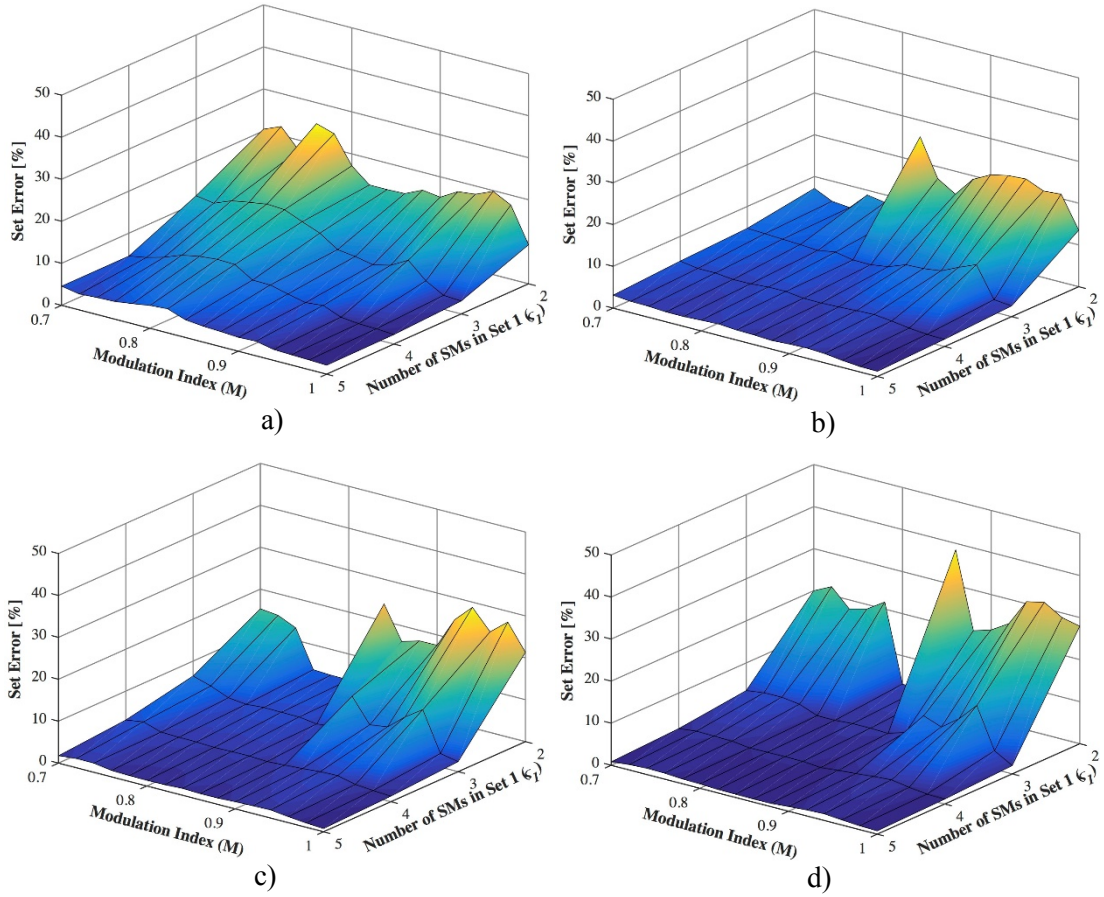


Fig. 5.25 Set Error where $\varsigma_3 = 2$ as a function of M and ς_1 for a) $\varsigma_2 = 2$ b) $\varsigma_2 = 3$, c) $\varsigma_2 = 4$, d) $\varsigma_2 = 5$

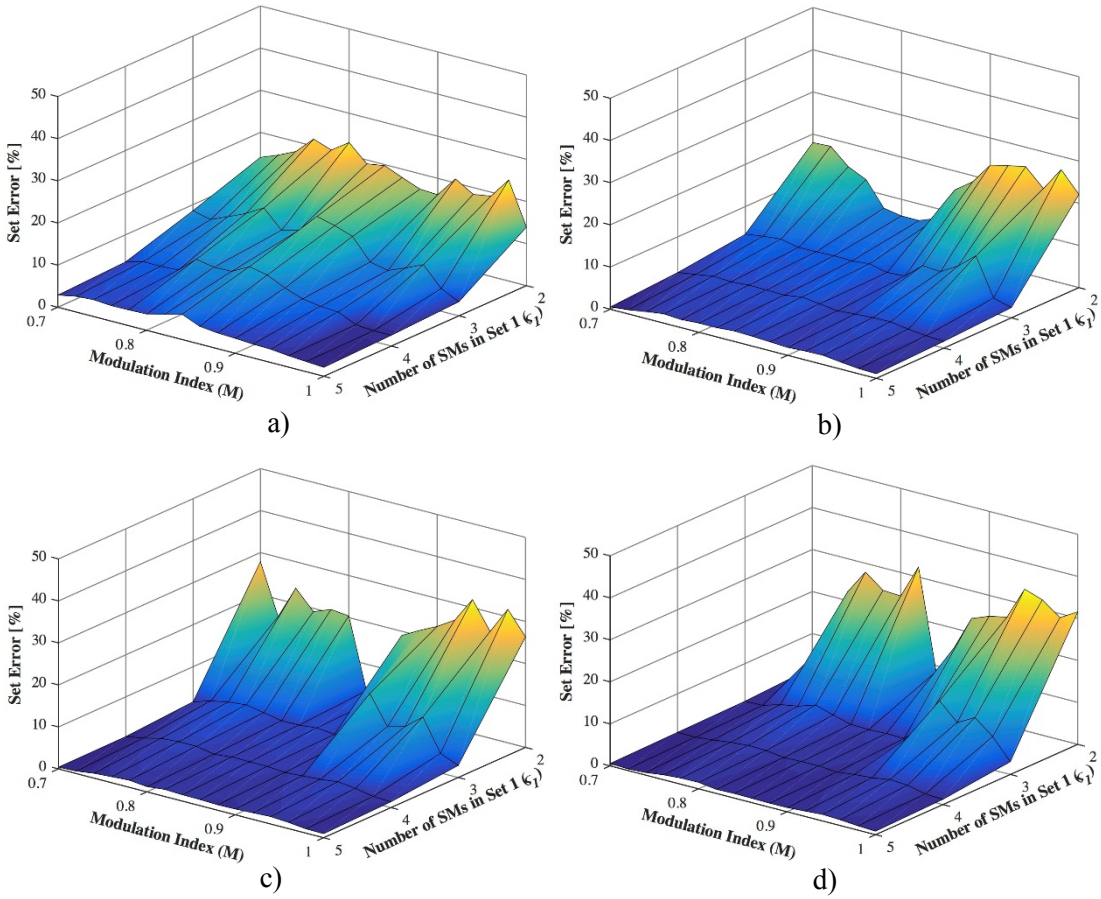


Fig. 5.26 Set error where $\varsigma_3 = 3$ as a function of *M* and ς_1 for a) $\varsigma_2 = 2$ b) $\varsigma_2 = 3$, c) $\varsigma_2 = 4$, d) $\varsigma_2 = 5$

The Set error is large and continues to increase in all cases when there are 2 SMs in S_2, although, the maximum error decreases as the number of SMs in S_3 increases. The Set error remains consistently high when $\varsigma_1 < 3$ and there is a clear spike yet again in the Set error when $\varsigma_1 = 3$ for all cases when $\varsigma_2 > 2$. There is now also a second spike present that becomes increasingly defined as ς_2 and ς_3 increases. The Set error becomes negligible when ς_1 and ς_2 are greater than 3 for all modulation indexes although the Set error is comparatively unaffected by ς_3.

When the Set error is plotted against SM_{min} for cases where $\varsigma_3 = 5$ and ς_2 ranges from 2 – 5 (Fig. 5.29a) – d)), it can again be seen that the error is greatest between 0.5 and 1.5 after which, it rapidly improves when $\varsigma_2 > 3$.

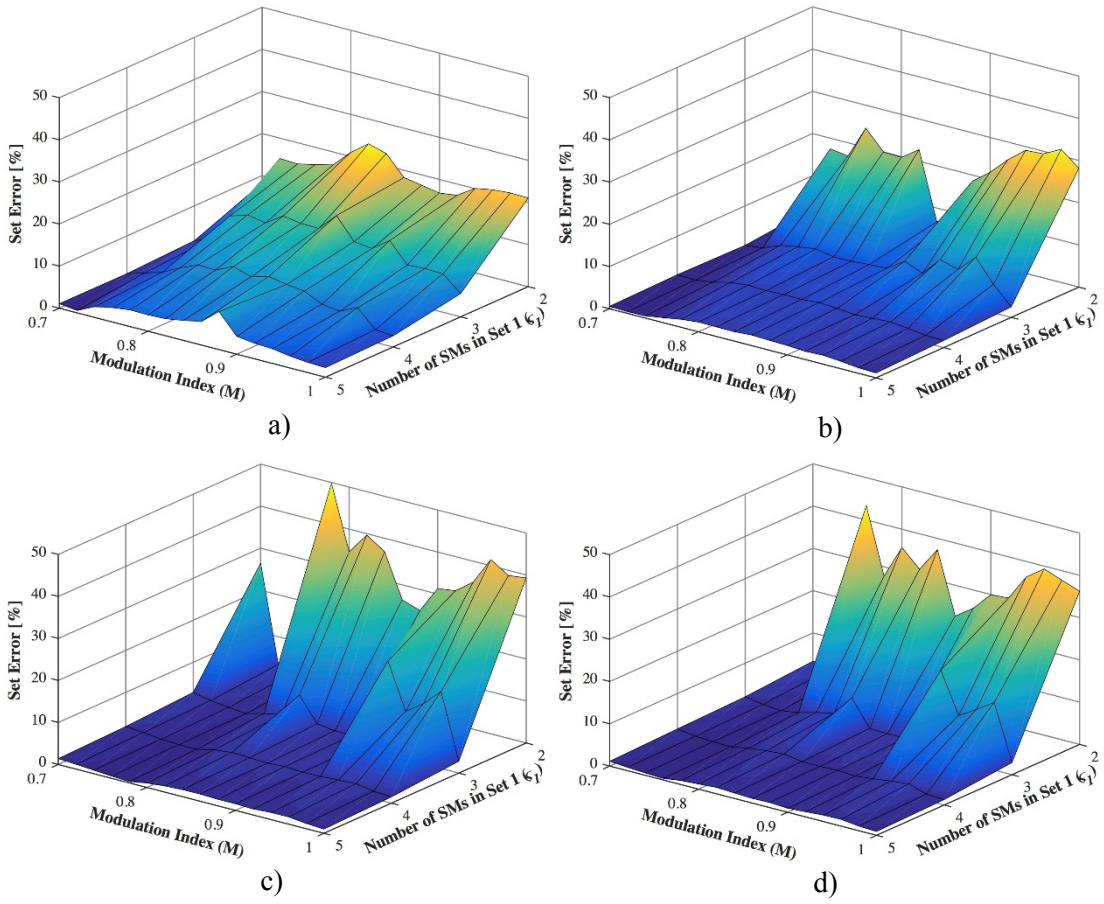


Fig. 5.27 Set error where $\varsigma_3 = 4$ as a function of *M* and ς_1 for a) $\varsigma_2 = 2$ b) $\varsigma_2 = 3$, c) $\varsigma_2 = 4$, d) $\varsigma_2 = 5$

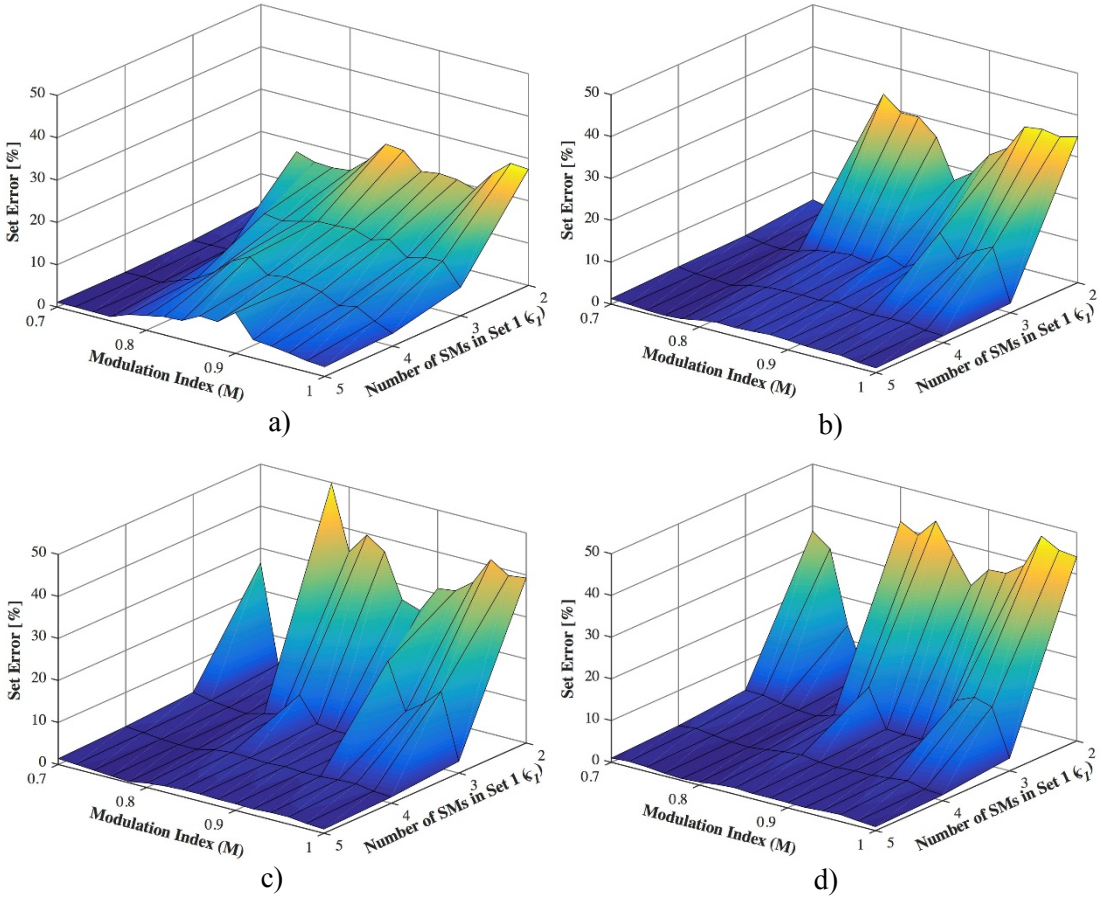


Fig. 5.28 Set error where $\varsigma_3 = 5$ as a function of M and ς_1 for a) $\varsigma_2 = 2$ b) $\varsigma_2 = 3$, c) $\varsigma_2 = 4$, d) $\varsigma_2 = 5$

In these cases, there is also a second spike when $SM_{min} = 3$ although this is smaller in magnitude. When $SM_{min} = 3$ there are two possible states, {3 0 0} and {1 1 0} where the number of SMs inserted per Set are displayed as $\{\varsigma_{on1}\ \varsigma_{on2}\ \varsigma_{on3}\}$. In the most extreme case, all the SMs in S_1 would charge while the other Sets remained at their constant value; this would create a very high error, so in most cases the HD-MMC algorithm selects the {1 1 0} case. With this option, both S_1 and S_2 charge equally and rise compared to S_3. With 4 or 5 SMs in S_2, the SMs in S_2 can be substituted for up to 2 SMs from S_3. HD-MMC algorithm can maintain a close balance between S_2 and S_3 however, only 1 SM from S_2 can be substituted for the SMs in S_1 and none from S_3. The HD-MMC algorithm therefore does not have enough redundancy for S_1 to maintain a stable voltage. The primary cause of the Set error can therefore be seen to be caused by S_1 when $\varsigma_2 > 3$ in Fig. 5.30.

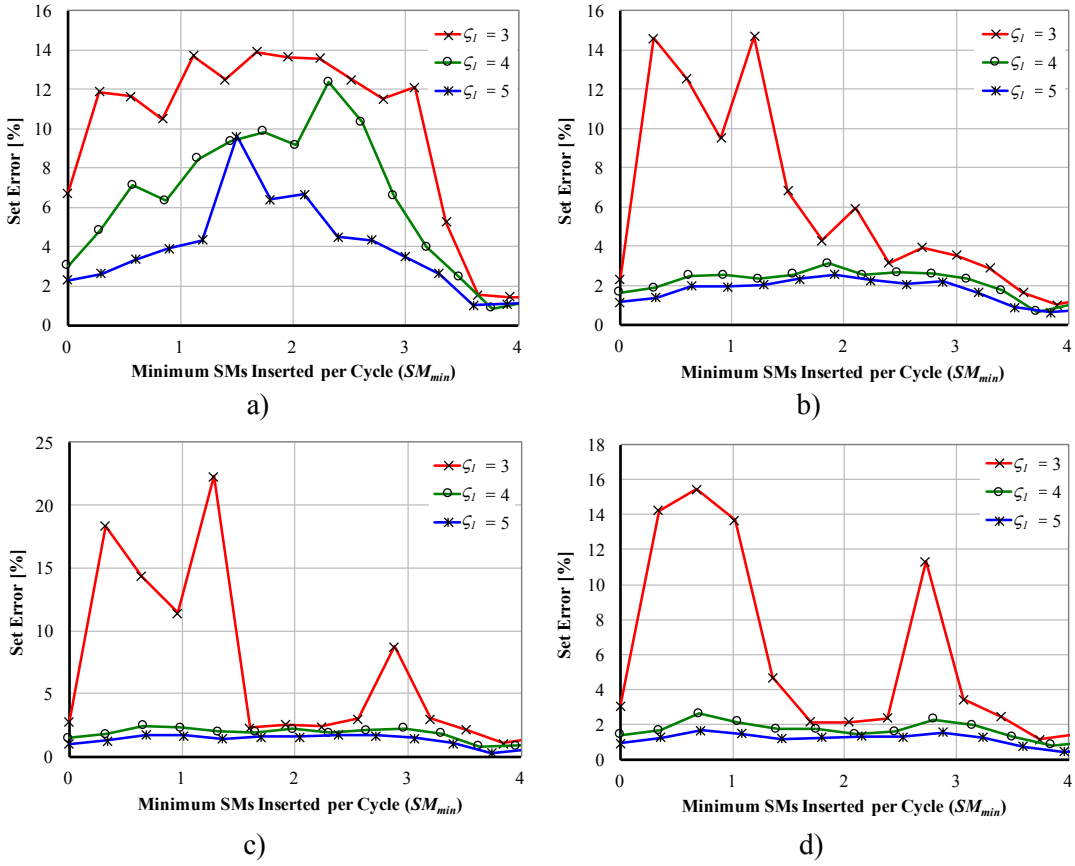


Fig. 5.29 Set voltage error vs. SM_{min} where $\varsigma_1 = 3$, 4 and 5 and $\varsigma_3 = 5$ with $U_r = [1\ 2\ 4]$ for a) $\varsigma_2 = 2$ b) $\varsigma_2 = 3$, c) $\varsigma_2 = 4$, d) $\varsigma_2 = 5$

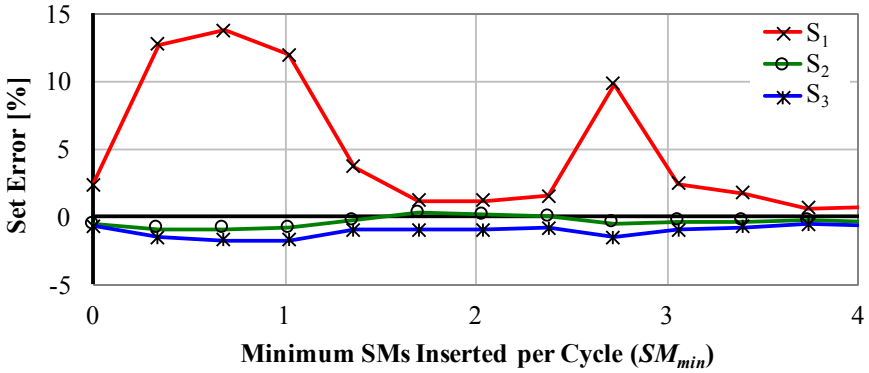


Fig. 5.30 The individual Set errors for the [3 5 5] converter configuration

The second spike appears earlier ($SM_{min} = 2$) when $\varsigma_2 = 3$, which can be seen to be primarily caused by S_2 rather than S_1 in Fig. 5.31 although, the error in S_1 is still high. At this point, the maximum current must be supported solely by 1 SM from S_2 or 2 SMs from S_1. In either case only one SM from the Set above can be replaced by the SMs in the selected Set which does not provide enough redundancy to balance the Sets. The Set error is also observed to be

universally poor when $\varsigma_2 = 2$ until $SM_{min} > 3.5$ and the maximum current can be shared between S_1 and S_2 or S_3. These results suggest that the Set error is primarily caused by a lack of redundancy between SMs in each Set with the limit given by:

$$u_{Sy} \geq 2u_{cy+1} \text{ or } u_{sy} \geq u_{cy+2} \tag{5.12}$$

whichever is lower.

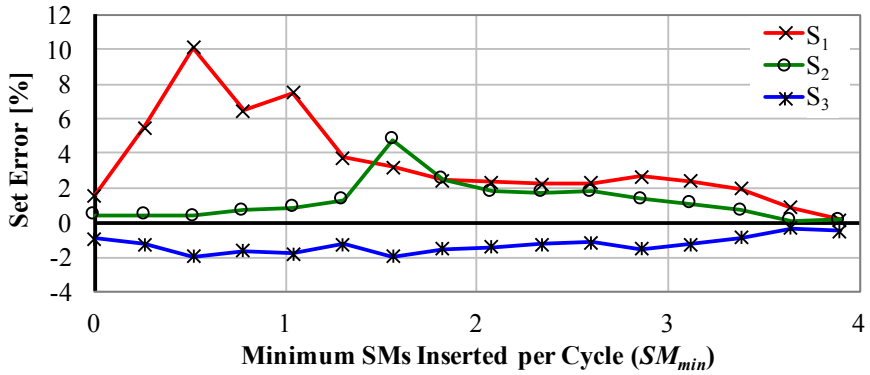


Fig. 5.31 The individual Set errors for the [3 3 5] converter configuration

If this is the case and the Set ratio is reduced, this should allow fewer SMs in the lower voltage Sets to be used. The graphs in Fig. 5.32a) – d) show the Set error for $U_r = [1\ 2\ 3]$ for ς_2 ranging from 2 to 5 and $\varsigma_3 = 5$. While the Set error remains high for $\varsigma_1 = 2$ and $\varsigma_2 = 2$ there is significant improvement for the $\varsigma_1 = 3$ and $\varsigma_2 = 3$ cases as predicted.

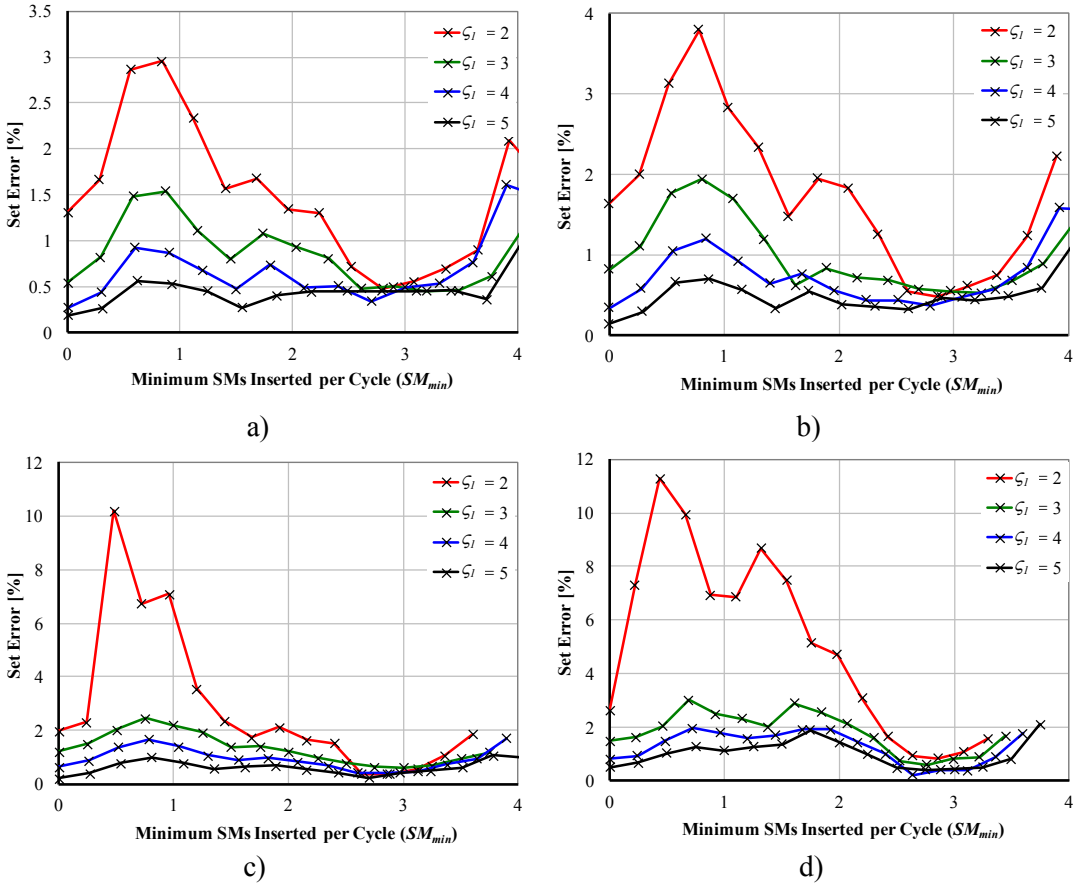


Fig. 5.32 Set voltage error vs. SM_{min} where $\varsigma_1 = 2$, 3, 4 and 5 and $\varsigma_3 = 5$ with $U_r = [1\ 2\ 3]$ for a) $\varsigma_2 = 2$ b) $\varsigma_2 = 3$, c) $\varsigma_2 = 4$, d) $\varsigma_2 = 5$

5.3 HD-MMC with Few SMs

While increasing the modules per Set improves the voltage drift, this places a significant limitation on the design of the converter. This may not affect HVDC applications where tens or hundreds of modules are used in each arm; however, one of the major benefits will be seen in converters with few modules per arm and hence a very high *THD*. An alternative approach is to reduce the power factor and hence move the peak arm current into a region where there is more Set redundancy. This reduces converter efficiency however, and so is only realistic in situations when a low power factor is required.

This section explores possible modifications to the HD-MMC algorithm to improve its performance when few SMs are available. One such method that is explored in detail involves increasing the number of redundant states through use of a targeted PWM strategy. Other possible strategies include, allowing the width of each step to be changed and use the circulating current to balance ensure the arm energies are equally balanced. These concepts

are briefly discussed but have not been fully developed and form part of the further work to be completed on this topic.

5.3.1 Hybrid HD-MMC

A modification to the Set control algorithm discussed in 4.1.2 is proposed and evaluated in this section to reduce the Set voltage deviation without limiting the operational range of the converter. This is achieved by artificially increasing the number of redundant states through use of high frequency PWM in Sets $S_2 - S_g$ with a 50% duty cycle. As a result, S_2 to S_g can output three levels: 0, 0.5 and 1. The options available in the selection matrix now follows (5.13) which is a significant increase from (4.6). For example, for a [3 3] converter the number of options are increased from 16 to 28 as shown in Table 5.3 when using the Hybrid HD-MMC concept. It is said to be a hybrid as it both increases the number of voltage levels and introduces an additional PWM generator to reduce the *THD*.

$$n_{st} = (\varsigma + 1)(2\varsigma - 1)^{g-1} \tag{5.13}$$

An example waveform resulting from the Hybrid HD-MMC selection matrix in Table 5.3 can be seen in Fig. 5.33. By including a PWM option, high voltage Sets have a half step option, generating additional redundancy and greatly reducing the Set voltage deviation even at a unity power factor. This can be seen by comparing the voltage deviations in Fig. 5.16 where the standard HD-MMC Set control is used, to Fig. 5.34.

Option	HD-MMC			Hybrid HD-MMC		
	S_{ON1}	S_{ON2}	U_{ref}	S_{ON1}	S_{ON2}	U_{ref}
1	0	0	0	0	0	0
2	1	0	1	1	0	1
3	2	0	2	2	0	2
4	3	0	3	3	0	3
5	0	1	2	0	1	2
6	1	1	3	1	1	3
7	2	1	4	2	1	4
8	3	1	5	3	1	5
9	0	2	4	0	2	4
10	1	2	5	1	2	5
11	2	2	6	2	2	6
12	3	2	7	3	2	7
13	0	3	6	0	3	6
14	1	3	7	1	3	7
15	2	3	8	2	3	8
16	3	3	9	3	3	9
17				0	0.5	1
18				1	0.5	2
19				2	0.5	3
20				3	0.5	4
21				0	1.5	3
22				1	1.5	4
23				2	1.5	5
24				3	1.5	6
25				0	2.5	5
26				1	2.5	6
27				2	2.5	7
28				3	2.5	8

Table 5.3 All the possible options for a [3 3] converter with the standard HD-MMC and Hybrid HVDC control

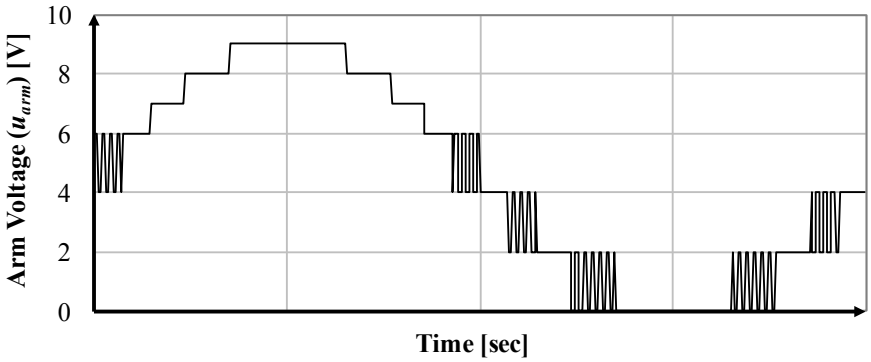


Fig. 5.33 Example arm voltage waveform resulting from the Hybrid HD-MMC Set control algorithm in a [3 3] converter

While the Hybrid HD-MMC algorithm resolves the Set balancing issue, it does so at the expense of an increased switching frequency and hence loss. For this reason, the added redundant steps created using the 50% PWM should only be utilised if the standard HD-MMC control fails the Set voltages. If this is enacted then the losses compared to the standard HD-

MMC converter can be reduced as shown in Fig. 5.35, as the circulating currents are smaller. The switching losses for the C-MMC are also included for comparison.

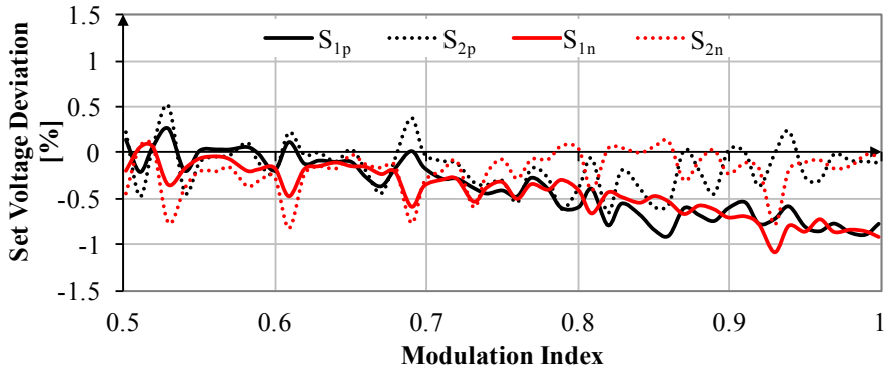


Fig. 5.34 Set voltage deviations for a [3 3] converter using the Hybrid HD-MMC Set control algorithm

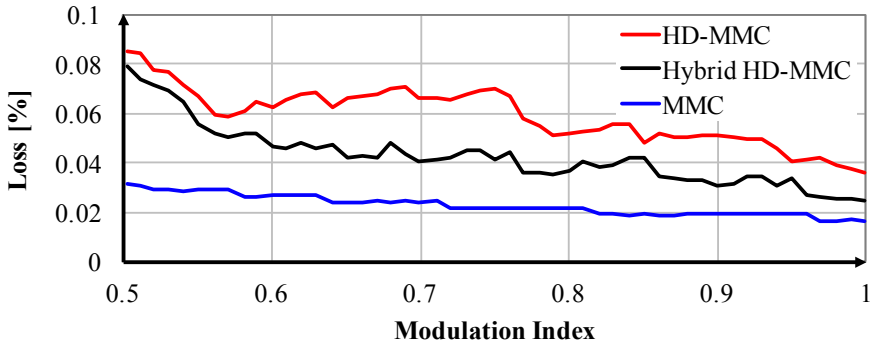


Fig. 5.35 Converter switching loss comparison between the Hybrid HD-MMC, HD-MMC and MMC

5.4 Chapter Summary

The aim of this chapter was to verify the HD-MMC under realistic running conditions and define its operating envelope. Through simulation in the MATLAB/Simulink environment, the HD-MMC algorithm was further verified in 3-phases with a closed loop control. Simulations at different weighting factors revealed that weighting factors greater than 2% had no longer reduced the switching frequency; however, the capacitor voltage ripple continued to rise. Interestingly, when the weighting factor was increased to 2%, the configuration of the two Set HD-MMC with the lowest switching frequency was the [4 14 0] configuration. As a result, it is possible to reduce the switching losses and the *THD* simultaneously. Compared to the C-MMC, the HD-MMC's switching losses rise quicker with respect to the operating frequency. The efficiency of the HD-MMC is therefore comparable to the C-MMC at 50 Hz however, it becomes less favourable towards 2,000 Hz.

An investigation into the operational limits of the HD-MMC found that more than three SMs per set were required to maintain converter stability for all operating conditions. Otherwise, if M was decreased such that one voltage level was omitted per cycle, the maximum (or minimum) arm current was consistently supported by the lowest voltage Set. An uneven energy distribution among the Sets was therefore created with insufficient redundancy rebalance the Set voltages. As this would limit the applicability and reduce efficiency of the HD-MMC, a strategy that could reduce the minimum number of SMs in the lower voltage sets was also proposed.

The key contributions of this chapter are therefore:

- The 3-phase verification of the HD-MMC algorithm with a closed loop control
- The weighting factor's influence on efficiency diminishes; however, the SM voltage ripple continues to rise, therefore only small weighting factors are necessary
- With the correct weighting factor, it is possible to simultaneously reduce the *THD* and increase efficiency
- As the operating frequency increases, the HD-MMC's efficiency compared to a C-MMC using NLM worsens.
- Four SMs are required in the lower voltage sets to maintain converter stability for all operating conditions
- There is no lower limit for the number of SMs in the highest voltage set
- The Hybrid HD-MMC algorithm can reduce the minimum number of SMs required to maintain converter stability

Chapter 6 Economic Evaluation of the Hybrid HVDC Transformer

The primary goal of the Hybrid HVDC Transformer concept is to reduce the capital cost of wind farms far from the PCC through elimination of the offshore AC and DC substations. These offshore substations have been reported to account for a significant proportion of the capital cost of the wind farm and so eliminating them has great potential to reduce costs. In eliminating the substations, the wind turbine costs will increase though, since additional converter modules and a more complex transformer must be incorporated into their design. As a result, to compare the conventional and Hybrid HVDC Transformer cases and verify that a cost reduction is achieved, the costs of each topology must be broken down to their constituent components. Such costs are not explicitly reported in the literature though, as this information is highly confidential and most published economic analyses have compared HVAC to HVDC where such a detailed breakdown of costs is not required.

To further complicate matters, Siemens have also proposed an alternative approach to the conventional HVDC wind farm topology. Here, the AC and DC substations are replaced by smaller DRU platforms to attempt to reduce costs and increase availability, reportedly representing a significant advancement from the status quo. Since it is a recent development however, few independent economic analyses of the DRU concept exist.

The DRU concept will reach the market before the Hybrid HVDC Transformer and if it proves popular, may be further developed to be co-located with an offshore wind turbine, eliminating the offshore platforms. It is this iteration of the DRU concept that the Hybrid HVDC Transformer is more likely to compete with and represents a fundamental difference in

philosophy, preferring simplicity over control. The potential cost reduction offered by eliminating these platforms is unclear however, and should be investigated.

The costs of a HVDC connected wind farm have therefore been deconstructed in this chapter to determine the price of the constituent components required for the Hybrid HVDC Transformer, DRU and next iteration of the DRU concepts. The capital cost of each concept is then compared to a conventional HVDC topology using a hypothetical 240 MW wind farm. This analysis considers the capital costs of each concept including the development, installation and component costs, the operational and decommissioning costs are not included.

The objectives of this chapter can be summarised as follows:

- Detailed breakdown of the capital cost of a HVDC wind farm, including the design, installation and component aspects.
- Independent economic analysis of the DRU concept compared to a conventional HVDC wind farm
- Potential cost reductions achievable through the next iteration of the DRU concept
- Economic analysis of the Hybrid HVDC Transformer
- Cost comparison of the Hybrid HVDC Transformer to conventional HVDC and alternative next generation wind farm topologies

The chapter is organised as follows; Section 6.1 describes the hypothetical wind farm and topologies of each configuration to be analysed. The costs of each topology are then calculated in Section 6.2 and analysed in Section 6.3. Finally, the key conclusions from this analysis are described in Section 6.4.

6.1 Hypothetical Wind Farm Topology

To properly evaluate the merit of the Hybrid HVDC Transformer, it should be compared not only to the conventional methods employed but also to systems that are likely to be used in the near future. To this end, a hypothetical 240 MW wind farm comprising 48 turbines separated by five diameters (5*d*s) in a uniform 8 by 6 rectangle has been considered and will be used to calculate the capital costs of four different transmission systems as shown in Fig. 6.1. The first system is a conventional layout with an AC transformer platform to step up the 33 kV AC inter-array voltage to HVAC. This is then converted to ±320 kV DC in the HVDC converter substation for transmission 100 km to shore. It is assumed that the wind turbines are all shunt connected on a single inter-array MVAC collection cable as shown in Fig. 6.1a.

The second topology has been proposed by Siemens to be used in round three wind farm projects and is described in Section 2.3.1. In this example, three DRU platforms have been

assumed with roughly a third of the turbines connected in parallel to each DRU substation (Fig. 6.1b) via a 66 kV AC collection grid.

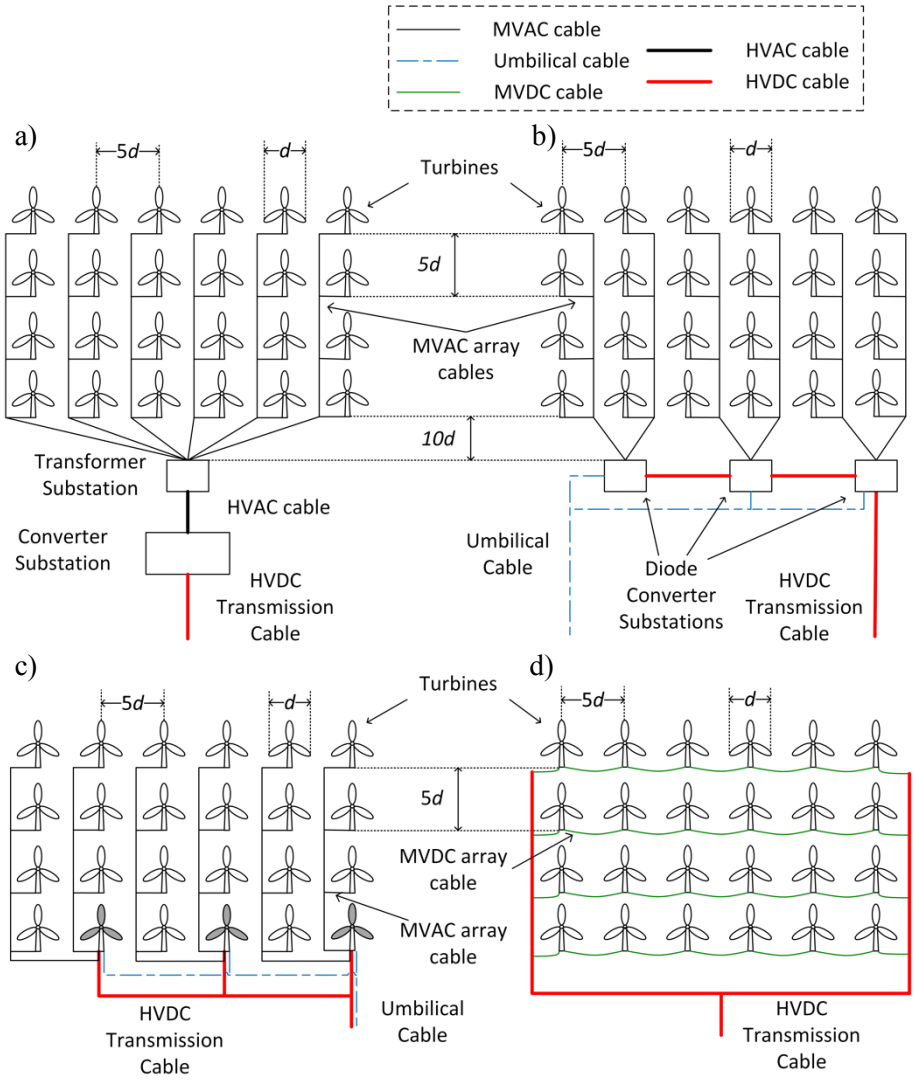


Fig. 6.1 Wind farm layouts for half the plant for each of the four designs, a) conventional HVDC, b) Diode platform, c) Diode integrated turbine, d) Hybrid HVDC

These platforms are reported to be similar in size to standard AC transformer substations and are connected in series to boost the DC voltage up to ±320 kV for transmission to shore. An umbilical AC cable from shore is also required to synchronise each AC grid on start-up but is isolated during normal operation.

A potential future iteration of the DRU concept where the diode platforms are supported by the foundations of the wind turbines is also considered. It is assumed that the foundations of large offshore wind turbines have enough redundancy to allow the addition of the diode

converters. These turbines (shown in grey in Fig. 6.1c) are then connected in series to boost the DC voltage up to the transmission level. An umbilical cable is still required for start-up.

These configurations are then compared to a wind farm using the Hybrid HVDC Transformer concept Fig. 6.1d. Here, five turbines are connected in series between the two HVDC transmission cables to boost the turbine voltage up to ±320 kV. Each row of five turbines is connected in parallel to the transmission cables, thereby ensuring a high degree of redundancy and eliminating the AC and DC substations. As the turbines utilise fully rated power electronics, no umbilical cable is required.

6.2 Cost Calculations

When investigating costs for wind farms, a wide range can be found in literature, particularly when the total cost is broken down into its constituent parts. This is primarily due to the difficulty in determining realistic prices in what is a fast moving and highly secretive industry but also because each wind farm is a bespoke design dependant on many factors. This analysis therefore uses several assumptions during the calculations which are listed and explained and are intended to provide a fair comparison between each topology in a theoretical design. This analysis only considers the capital costs, including the design, installation and individual component costs.

As illustrated in Fig. 6.2, the cost of all the constructed HVDC offshore wind farms has been proportional to their rated capacity [14], [158]–[160][15], [159]–[161]. Therefore, the cost of the hypothetical 240 MW can be estimated to be in the region of £1,020M. This reference cost was required as several sources give the cost of plant components as a percentage of the wind farm's cost. Using this indicative cost, the percentage costs can be converted to their monetary value.

From the technical appendix of The National Grid's ten year statement [11], the cost of a VSC for offshore use is approximately £0.8M and is assumed to increase linearly with power rating. It is therefore estimated at £30M for 240 MW with a ±320 kV transmission line. IGBTs are estimated to contribute to around 70% of the VSC cost and diodes are assumed to cost 40% of the price of an IGBT.

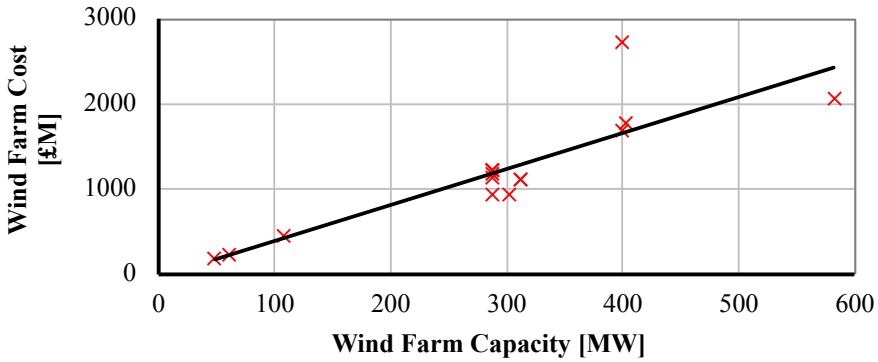


Fig. 6.2 Cost and capacity of completed German offshore wind farms [14], [158]–[160][15], [159]–[161]

Siemens' proposed concept utilises a 66 kV inter-array cable and this was found to be €200/m in a DNV GL report [162]. Using the same exchange rate as was used to calculate the wind farm cost, gives a cable cost of £146/m. These general plant costs are summarised in Table 6.1.

Element	Cost	Unit
Plant Cost	1020	£M
Farm Rating	240	MW
Turbine Rating	5	MW
Rows	8	
Columns	6	
Number Turbines	48	
Hybrid Cluster	6	
Blade Diameter	200	m
Turbine Spacing	5	Diameters
Distance to Substation	2	km
Distance to PCC	100	km
Tower Height	0.05	km

Table 6.1 General costs for a 240 MW offshore wind farm based on the Meerwind Sud/Ost project

From [163] it is known that 33% of a wind farm's cost can be attributed to the turbine nacelles, which includes the generator and the mechanical and electrical drive train. Within the electrical drive train, 5.01% is attributed to the DC/AC converter and 3.59% to the transformer. For the first 3 scenarios, all this equipment remains unchanged however, for the Hybrid case, the transformer is estimated to be 50% more expensive to account for the more complicated MF design. It also has an additional AC/DC stage, which is normally located on the HVDC platform. If it is assumed splitting the VSC into smaller blocks will not increase the cost then this should be equal to roughly 2.5% of the total wind farm cost. This is a reasonable cost as the smaller SMs will likely lead to economies of scale and result in a less complicated design.

In the third scenario, where the diode platform can be integrated into the wind turbine foundations, additional components are required. This includes diodes which are considered

to be 60% cheaper than IGBTs, giving the converter price as £7M for the farm, switch gear at roughly £0.15M and £2M for reactors [11] to balance the reactive power within the AC grid. The costs of the tower, foundation and installation costs of the turbines are given by [163] as a percentage of the total farm costs. It is assumed here that the weight difference due to the added converter stage in scenario 4 or diode converter from scenario 3 is within tolerance for the turbine design conditions. This is particularly valid for the Hybrid case, as operating in the MF range will greatly reduce the weight of the transformer, hence offsetting, at least in part, the added weight of the converter. According to the Siemens literature [164], the diode converter can be passively cooled and so there is no cost associated with this. In the Hybrid case, any cooling that may be required is assumed to be provided by the existing cooling systems in the nacelle and so no additional costs are included. The costs associated with the turbines are summarised in Table 6.2.

	Standard	Diode Platform	Diode Turbine	Hybrid	Unit
	Turbine Nacelle				
Total	33%	33%	33%	33%	Of Farm
DC/AC	5.01%	5.01%	5.01%	5.01%	Of Turbine
Transformer	3.59%	3.59%	3.59%	3.59%	Of Turbine
	0	0	0	150%	Increase
AC/DC	-	-	-	96	£M
	-	-	-	8.92%	Of Farm
Adjustment	0%	0%	0%	10.7%	Of Turbine
	Diode Section				
Converter	-	-	96	-	£M
	-	-	70%	-	Of VSC
	-	-	40%	-	Of IGBT
	-	-	8	-	£M
Switch Gear	-	-	0.17	-	£M
Reactor	-	-	1.15	-	£M
Adjustment	-	-	3 %	-	Of Turbine
	Tower				
Cost	8%	8%	8%	8%	Of Farm
	Foundation				
Cost	15%	15%	15%	15%	Of Farm
	Installation				
Cost	9%	9%	9%	9%	Of Farm
Total	**636**	**636**	**645**	**670**	**£M**

Table 6.2 Cost break down of a 5 MW turbine including the tower, foundation and installation costs

The National Grid's ten year statement [11] gives the cost of a 200 – 400 MW AC platform transmitting at 220 – 275 kV as £30 – £40 million. By iterating between the two power levels, the cost for the AC platform is estimated to be £40 million. Similarly, the DC converter platform is quoted at £400 - £490 million for a 1000 MW 320 – 400 kV transmission line platform. As the farm is rated at 240 MW, cost of the converter station is assumed to be 76% less than that quoted, giving it as £100 million for the top side (assumed to include converter

hardware) and the jacket. The installation costs of the platforms are given in [163] as 0.5% and 1.3% of the farm costs for the AC and DC platforms respectively for the topside and foundation. In the case of the Diode Platform, the literature refers to the converter being placed on an AC platform [164]. If the component costs of the platform (transformer, cooling, reactor, switch gear) are subtracted from its total cost, the structural cost can be estimated. The cost of the three platforms can then be calculated by adding the diode cost to the structural, switch gear and reactor costs as shown in Table 6.3.

	Standard		Diode Platform	Diode Turbine	Hybrid	Unit
	Quantity					
Number	1	1	3	0	0	-
	Top Side & Jacket					
Type	AC	DC	Diode	-	-	-
Converter	-	-	8	-	-	£M
Transformer	3.75	-	3.75	-	-	£M
Cooling	2 %	-	2 %	-	-	Of Platform
Switch Gear	0.17	-	0.17	-	-	£M
Reactor	1.15	-	1.15	-	-	£M
Structure (alone)	33.64	-	33.64	-	-	£M
1 Unit	39.5	100	39.5	0	0	£M
	Installation					
Topside	0.5%	1.3%	0.5%	-	-	Of Farm
Foundation	0.5%	1.3%	0.5%	-	-	Of Farm
Sub Total	49.28	125.43	120.08	N/A	N/A	£M
Total	174.71		120.08	0	0	£M

Table 6.3 Cost break down of the offshore substations required in each scenario

The turbines are assumed to be set out in a 10 by 5 grid and separated by 1 km to mitigate wake interactions. From Fig. 6.1 the number of inter-array cable links can be seen for each of the scenarios. It is also assumed that 2 km of cable is required for each offshore platform. In Scenarios 3 and 4, DC collection cables are also required and these are assumed to be at the same rating as the transmission cable. The inter-array cable costs are summarised in Table 6.4.

In the case study the transmission line is 100 km from the export point within the farm to the PCC onshore. Any additional HVDC cable required for collection purposes, e.g. in scenario's 3 and 4, are classed as DC collection cables and are accounted for within the inter-array cable section. The unit cable cost has been extrapolated from the given costs for an extruded 320 kV cable between 600 – 2000 MW. This gave a unit cost of £0.2 million/km. The cables were assumed to be installed in two separated trenches 10 m apart and the average cost quoted was £0.5 million/km as shown in Table 6.5.

	Standard	Diode Platform	Diode Turbine		Hybrid		Unit
	Type						
AC/DC	AC	AC	AC	DC	DC	DC	-
Category	Array	Array	Array	Collection	Array	Collection	-
Rating	33	66	66	320	320	320	kV
	Length						
Turbine Span	42	42	45	8	40	19	km
Turbine Distance	1	1	1	1	1	1	km
Station Distance	15.53	12.37	0	0	0	0	km
Total	57.53	54.37	45	8	40	19	km
	Installation						
Unit Cost	0.79	0.79	0.79	0.85	0.85	0.5	£M/km
Cost	45.4	43	35.6	6.8	34	9.5	£M
	Cable						
Unit Cost	0.35	0.09	0.09	0.16	0.06	0.16	£M
Cost	20.23	4.87	4.03	1.24	2.26	2.95	£M
Total	**65.68**	**47.82**	**47.62**		**48.7**		**£M**

Table 6.4 Inter-array cable costs for each scenario

In the diode converter scenarios, an additional umbilical cable is required to provide power to the AC grid and the turbines to allow a black start as the diode converter is unidirectional. As it is to connect to a 66 kV grid and it is only used during start-up, a 66 kV inter-array cable has been used here. In [164] it is claimed that the umbilical cable cost will have only a minor impact on the overall cost due to collaboration with a transmission cable company. It is therefore assumed that the cable can be laid in the same trench as the transmission cable, or at least for no additional cost. Its installation costs are therefore assumed to be zero.

	Standard	Diode Platform		Diode Turbine		Hybrid	Unit
	Type						
	HVDC	HVDC	Umbilical	HVDC	Umbilical	HVDC	-
	Length						
Cable Distance	200	200	100	200	100	200	km
	Installation						
Unit Cost	0.85	0.85	0	0.85	0	0.85	£M/km
Cost	85	85	0	85	0	85	£M/km
	Cable						
Unit Cost	0.16	0.16	0.146	0.16	0.146	0.16	£M/km
Cost	31.03	31.03	14.6	31.03	14.6	31.03	£M
Total	**115.12**	**126.53**		**126.53**		**115.12**	**£M**

Table 6.5 Transmission cable costs

At the PCC the same standard HVDC converter and AC transformer stations are used to link the transmission cable to the grid. These have been reported to be 2% and 0.7% of the wind farm's cost respectively as shown in Table 6.6. Clearly this is considerably cheaper than the offshore structures largely due to the reduced structural cost of the substations. There is also reportedly a 4% development cost for the wind farm.

	Standard	Diode Platform	Diode Turbine	Hybrid	Unit
	Onshore Platforms				
HVDC	2%	2%	2%	2%	Of Farm
AC	0.7%	0.7%	0.7%	0.%	Of Farm
Foundation	1%	1%	1%	1%	Of Farm
Total	36.186	36.186	36.186	36.186	£M
	Development				
Cost	4 %	4 %	4 %	4 %	Of Farm
Total	**39.12**	**39.12**	**39.12**	**39.12**	**£M**

Table 6.6 Additional costs

6.3 Economic Analysis

The conventional wind farm cost can be seen in Fig. 6.3 to have the highest cost at around £1.1 billion. Examining a more detailed breakdown of its costs reveals that around 16% is attributed to the AC and DC offshore substations required to transform the power for transmission. According to these results, replacing the AC and DC offshore substations with three diode substations and switching to a 66 kV inter-array cable reduces the cost by around 4 %. This scenario still requires three platforms to be constructed and installed and while considerably smaller and simpler than the HVDC platform, is still expensive. If the diode substation could be reduced in size such that it could be collocated with the wind turbine using the same foundations, the cost could be reduced by around 15 %. To achieve the size reduction the power rating of the converter would likely need to be reduced, resulting in more, smaller platforms. If, however, three platforms connected in series are still required to reach the transmission level voltage, some of these additional converters would need to be connected in parallel. This would further complicate the turbine control.

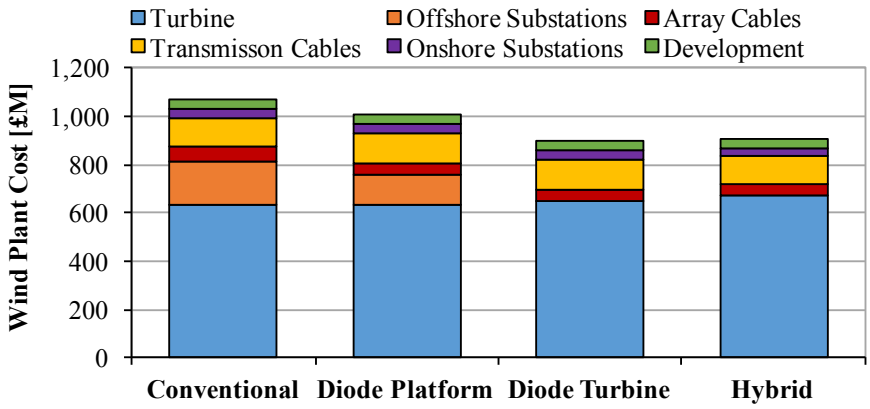


Fig. 6.3 Total cost breakdown for the conventional, diode platform, diode turbine and hybrid wind farm topologies

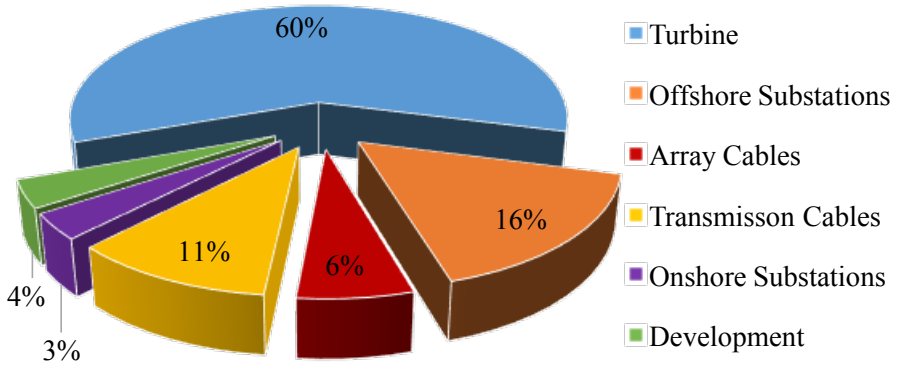


Fig. 6.4 Complete Cost breakdown of a wind farm using a conventional HVDC topology

The Hybrid transformer achieves a 13% cost reduction by eliminating the HVDC substation; however, the turbine cost does increase by 5% as shown in Fig. 6.3. This is due to the more expensive transformer and also the VSC units from the HVDC substation being moved to the turbine. The cabling cost (DC collection cable) also increases, as a fully rated HVDC cable must extend to the far end of the farm.

A more detailed cost breakdown of the Hybrid Transformer scenario is given in Fig. 6.5 where the wind turbine now accounts for 75% of the wind farm costs compared to only 62% in the conventional case (Fig. 6.4). This could be advantageous as many turbines are used to create the farm and so there is a large inherent redundancy and may also be subject to economies of scale. Furthermore, turbines can be thoroughly tested to reduce their chance of failure and increase investor and insurer confidence, thereby further reducing the overall cost of the farm.

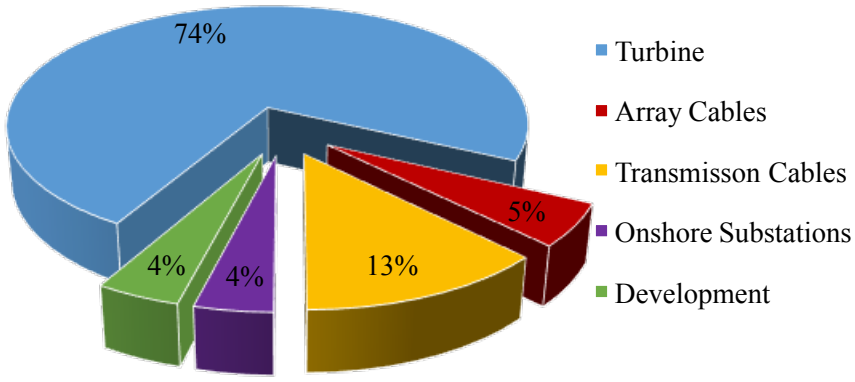


Fig. 6.5 Complete Cost breakdown of a wind farm using the Hybrid HVDC Concept

6.4 Chapter Summary

The aim of this chapter was to provide an economic analysis of the Hybrid HVDC Transformer in the context of both existing and potential future HVDC wind farm topologies. To this end a hypothetical, 240 MW offshore wind farm with 48 turbines arranged in an 8 by 6 grid formation was devised. The capital cost of this wind farm was then calculated assuming four different connection topologies. These included a conventional HVDC connection, the DRU, a further iteration of the DRU and Hybrid HVDC Transformer concepts. Through analysis of multiple sources, the constituent components of each topology were derived and summed to reveal their respective capital costs.

The DRU concept was found to reduce the capital costs by 5.7% compared to the conventional layout. Further improvements are possible if the DRUs are collocated with the wind turbines, resulting in a 16.1% reduction in cost. The Hybrid HVDC Transformer concept results in a similar cost reduction at 14.7%. While this is slightly lower than the potential next iteration of the DRU it does provide the wind farm operator with additional control of the wind turbines. This additional control is also likely to result in a more stable offshore network.

The key contributions of this chapter are therefore:

- A detailed breakdown of the component costs of an offshore HVDC wind farm
- An economic analysis of the DRU concept
- An economic analysis of an extension of the DRU concept
- An economic analysis of the Hybrid HVDC Transformer

Chapter 7 **Conclusions**

This thesis has presented the Hybrid HVDC Transformer concept. Located within each wind turbine nacelle or tower, it steps up the internal DC bus voltage for transmission directly from the turbine. The offshore HVDC and AC substations are therefore not necessary, increasing redundancy and reducing the capital cost of the wind farm. In seeking to optimise the Hybrid HVDC Transformer's configuration, the HD-MMC control algorithm was created. The HD-MMC creates additional voltage levels for a given MMC configuration, reducing the generated *THD*. This was shown through physical experiments to be more efficient than using PWM for converters where the number of SMs is restricted. The proposed HD-MMC therefore has many applications in addition to the Hybrid HVDC Transformer particularly in the MV and LV markets. These include, but are not limited to, grid services such as those provided by STATCOMs or DC/DC converters in solar plants where the HD-MMC could reduce the switching losses. The HD-MMC is also well suited to the electric vehicle and aerospace industries, where space is restricted. Reducing the generated *THD* would therefore allow for a smaller filter.

This chapter summarises the work presented in this thesis to fulfil the following research objectives:

- Assessment of core loss equations for non-sinusoidal waveforms based on usability and accuracy
- Comparison of converter topologies to determine suitable configuration for the Hybrid HVDC Transformer
- Development of an analytical loss model to compare different Hybrid HVDC Transformer Configurations and determine key requirements
- An economic assessment and comparison of the Hybrid HVDC Transformer to conventional HVDC collection systems and new approaches proposed by industry.

- Development of a novel High Definition MMC (HD-MMC) control algorithm to improve the performance of the MMC in LV and MV applications.
- Experimental validation and assessment of the HD-MMC.
- Optimisation and operational range of the novel control strategy.

Furthermore, the next steps to develop both the HD-MMC algorithm and Hybrid HVDC Transformer are discussed.

A summary of the Hybrid HVDC Transformer is presented in Section 7.1, including the overall offshore grid layout and economic analysis. The HD-MMC algorithm is then discussed in Section 7.2, including the impact of the experimental results and potential mitigation methods. Finally, the planned future works concerning the Hybrid HVDC Transformer and HD-MMC control algorithm are outlined in Section 7.3.

7.1 Hybrid HVDC Transformer Summary

A detailed literature review was conducted in Chapter 2 including a preliminary analysis of the major converter topologies and transformer configurations available in the literature. Solid state (non-magnetic) DC/DC transformer topologies were considered as they do not require any large, complicated magnetic components but were ultimately dismissed, due to their non-modular construction and limited step-up ratios. This left magnetic transformer topologies, of which the single core, 3-phase configuration of the E-core made most efficient use of the limited space available. The five major converter topologies including the FB, NPC, FCC, CHB and MMC were considered for the inverter and rectifier to be connected to the primary and secondary sides of the magnetic transformer. Of these, the FB and MMC showed most promise and hence were considered for further investigation.

Simulation models of three Hybrid HVDC transformer configurations were created in the MATLAB/Simulink environment. In the first, both the primary and secondary side converters used the FB topology (FB-FB), a second configuration used the MMC for both primary and secondary sides (MMC-MMC). The final configuration explored the possibility of combining the FB and MMC topologies, using the FB on the primary and the MMC on the secondary (FB-MMC). These models were used to simulate the converters and link with a mathematical model of the magnetic transformer components. The mathematical model was updated and optimised for each configuration of the converter topologies and for each operating frequency modelled (500 – 2,000 Hz). This was done as the waveform shape generated by the converter topology and its operating frequency, influences the peak winding current and core flux density considerably. To fully evaluate the impact the configuration and operating frequency

have on the performance and volume of the Hybrid HVDC Transformer, the magnetic design needed to be adjustable.

7.1.1 Summary of the Available Core Loss Equations

While the SE has been extensively used over the past century to calculate the magnetic transformer core loss, it is only applicable to sinusoidal waveforms. To accurately calculate the core loss created by each converter configuration, another loss equation was selected. There exists a litany of methods in literature that can be used to calculate the core losses due to non-sinusoidal waveforms generated by power electronic converters. Despite this, industry frequently persists with the SE, using the Fourier Transform to convert the waveform to its sinusoidal components. Theory suggests this to be inapplicable however, due to the non-linearity of the SE.

To calculate the core loss in the Hybrid HVDC Transformer, three methods were evaluated based on their ease of use and accuracy. The iGSE was selected from the literature as it provided the best trade-off between accuracy and ease of use, with all necessary parameters calculable from common parameters provided by core manufacturers. This was compared to the original SE as a control and FTSE. Voltages with different profiles were applied to a physical transformer core; these include sinusoidal, triangular, distorted sinusoidal, 50% duty square wave and 33% duty square wave over a range of frequencies and flux densities. The transformer core was placed in an environmental chamber and the primary winding voltages and currents measured under no load to calculate the core loss. The losses were then calculated using the SE, FTSE and iGSE and compared to the measured core loss to determine their respective accuracy.

All three core loss calculation methods performed best when the core was excited using a sinusoidal waveform. While the FTSE proved relatively accurate for the triangular and distorted sinusoidal waveforms, its accuracy dropped significantly for the square wave cases. The iGSE proved the most accurate overall, especially in the square wave cases. While the effects of relaxation were not readily observed when comparing the 50% to 33% duty square waves, it may become more appreciable in higher switching frequency situations (PWM). As a result, the iGSE was selected to calculate the core losses created by the waveforms generated by the transformer converters.

7.1.2 Summary of the Hybrid HVDC Transformer Topology Comparison

With the core loss equation selected, the magnetic transformer model could be finalised and combined with the converter simulation models for the FB-FB, FB-MMC and MMC-MMC configurations. The results of the combined model showed that the switching losses dominated Hybrid HVDC Transformer configurations utilising the FB converter. This was due to the high frequency PWM switching, leading to the conclusion that PWM should be avoided wherever possible in the MF range. The lower switching frequency operation of the MMC-MMC proved the most significant consideration in the topology design resulting in considerably lower losses. While the volume of the FB-FB topology was marginally smaller than that of the MMC-MMC, the FB-FB losses were too large to be realistically considered.

In addition to the converter configuration, the number of turns on the primary winding (keeping the transformer ratio constant) was also investigated. This also proved to have a significant effect on both the efficiency and volume of the Hybrid HVDC Transformer. While increasing the number of primary winding turns significantly reduces the core losses, each additional turn yielded a decreasing return; however, the winding losses continue to increase. As a result, the combined magnetic transformer losses reach a minimum with six primary winding turns and begin to rise thereafter.

The Hybrid HVDC Transformer losses were found to increase with frequency while its volume decreased. The increase in losses, primarily driven by the rising converter switching frequency, rose relatively linearly; however, the law of diminishing returns applied to the volume reduction.

The most significant observation to come out of the Hybrid HVDC Transformer optimisation was the necessity to avoid PWM in the MF range. Even using the MMC-MMC case, PWM is still necessary for the primary side converter due to the limited voltage range supplied by the MVDC bus. This led to the development of the novel HD-MMC algorithm, to create additional voltage levels without increasing the number of SMs in the MMC.

7.2 HD-MMC Summary

7.2.1 HD-MMC Algorithm Summary

The analysis of the Hybrid HVDC Transformer revealed that avoiding PWM operation is highly desirable when operating in the MF range, not only to reduce losses but also volume. The low voltage MMC is restricted in the number of SMs and hence voltage levels that it can

create. As a result, without overrating the MMC by adding additional SMs, the generated harmonics will be too high. This is a problem not only for the Hybrid HVDC Transformer but also for other MV and LV MMC applications where PWM would be necessary.

To achieve this, Chapter 4 introduced the novel HD-MMC algorithm, capable of increasing the number of voltage levels that can be created by any given MMC. This is done by repurposing some of the redundant states that exist in the MMC and hence make more efficient use of the existing hardware. To accomplish this, the SMs within each arm are grouped into Sets, with the SMs within a given Set charged to the same voltage and different from the other Sets in the arm. By carefully selecting which SMs to switch in, additional voltage levels are created. Balancing of the Set voltages is achieved through the HD-MMC algorithm and by introducing Set redundancy by intelligently selecting the ratios between the SMs between each Set.

The HD-MMC algorithm can be easily integrated into the existing control strategy employed by the MMC, thereby providing a minimal intrusion and simplifying implementation. While the analysis in this chapter has focused on the half bridge MMC topology, the HD-MMC algorithm is also applicable to other more modern MMC topologies including the full bridge MMC.

It was shown that as the number of Sets and SMs within each Set increases, the number of possible combinations also rises and quickly presents a multivariable optimisation problem. Simplistic methods that only consider the impact on one Set voltage, i.e. the Set with the highest voltage deviation from nominal, often fail to select the best option. This led to large Set voltage deviations and hence increased *THD* and converter losses. By considering the impact that a choice has on all the Set voltages a significant performance improvement can be realised.

7.2.2 HD-MMC Experimental Validation Summary

To validate the HD-MMC algorithm, an experiment was devised in collaboration with SINTEF in Norway and IREC in Spain. SINTEF have built three MMCs for use in experiments including the 18 SM, half bridge converter used for the validation. Three different HD-MMC configurations were investigated, [9 9], [5 13] and [3 15] SM distributions using NLM and were compared to an 18 SM C-MMC using NLM and PWM. The different converter topologies were evaluated based on the *THD* produced and the switching frequency. The

overall converter efficiency, arm currents and SM voltages were also measured to validate the correct operation of the HD-MMC algorithm.

To focus the results solely on the performance of the HD-MMC algorithm, the converter was operated using an open loop control without a CCS controller. To further simplify the experiment, only one phase of the converter was used. The external power and CCS control blocks were omitted from the validation as these create additional harmonics especially when they are not tuned properly. As a result, the injected harmonics from the outer control would likely be different for each topology as the outer control cannot be tuned to provide an equal performance for each configuration. While omitting the outer control and operating in single phase does not provide a realistic scenario, these omissions should not influence the success of the HD-MMC algorithm.

The results showed that the HD-MMC algorithm successfully balanced the SM voltages and consistently generating the correct levels. As with the C-MMC, the arm current of the HD-MMC contained a large second harmonic since no attempt was made to cancel it. The HD-MMC's *THD* was roughly similar to the PWM C-MMC and significantly lower than the NLM C-MMC. While the switching frequency of the HD-MMC was marginally higher than that of the NLM C-MMC, it was significantly less than the PWM C-MMC. While the overall converter efficiency was measured, its accuracy is questionable which is why the number of switching events was counted.

In addition to the five cases described above, the experiment also documented the impact of a weighting factor applied to the SM balancing controller. This weighting factor influences how the SMs are sorted based on whether they are already switched in or not. Consequently, the weighting factor impacts both the switching frequency and the SM capacitor voltage ripples. Higher weighting factors resulted in significantly lower switching frequencies but often also a slightly higher *THD*, which is likely a result of the larger capacitor voltage ripples.

7.2.3 Summary of the 3-Phase Evaluation of the HD-MMC Algorithm

With the HD-MMC control algorithm verified experimentally, a detailed 3-phase model was created in the MATLAB/Simulink environment to allow for further analysis. Using this model, the HD-MMC's performance with closed loop control could be verified and compared to that of the C-MMC with the same number of SMs and the same number of voltage levels. This showed that the HD-MMC algorithm continued to perform as expected in 3-phases and with full closed loop higher level control.

Increasing the weighting factor from 0 to 2% was shown to greatly reduce the number of switching events for each case. Above 2% the weighting factor had relatively minimal effect on the switching losses; however, the SM capacitor voltage ripple continued to increase. The optimum weighting factor is therefore found to be around 2%. At higher values, the capacitor voltage ripple continues to rise, reducing converter stability and increasing output *THD* for little reduction in switching loss.

The efficiency of the [4 14 0] HD-MMC was compared to the [18 0 0] and [32 0 0] C-MMC configurations at operating frequencies ranging from 50 – 2000 Hz. This showed that the switching losses rose linearly with operating frequency. The HD-MMC switching losses increased quicker with frequency than either C-MMC case. Consequently, there will be an operating frequency where it will be more efficient to overrate the converter by inserting additional SMs than use the HD-MMC algorithm.

7.2.4 Summary of the Operational Range of the HD-MMC

The operating range of the HD-MMC was also explored. To do this, a [3 3] HD-MMC was run at power factors ranging from 0 to 1, modulation indexes 0.7 to 1 using NLM and PWM with carrier frequencies ranging from 150 to 1150 Hz. The carrier frequency was found to have a negligible influence on the Set voltage error but the modulation index and carrier frequencies were found to influence converter stability. The converter performed well over the majority of modulation index and power factor combinations; however, when the power factor was close to unity and the modulation index close to 1, it became unstable.

The Set voltage stability increases significantly if four or more SMs are in each Set, although this places a lower limit on the number of SMs in each arm of eight. Increasing the number of voltage levels generated has the greatest impact when few voltage levels were generated originally. Therefore, it stands to reason, that the HD-MMC has the greatest potential in applications where the number of SMs in each arm is significantly constrained. Limiting the HD-MMC algorithm to topologies where each arm must have a minimum of 8 SMs therefore may significantly reduce its potential market.

7.2.5 Summary of Potential Extensions to the HD-MMC Algorithm

An extension to the HD-MMC algorithm was therefore proposed. The Hybrid HD-MMC algorithm proposed using high frequency switching to create a virtual voltage level, similar to

PWM. This significantly increased the redundant states available and resulted in a significant Set voltage stability improvement at the cost of an increased switching frequency.

7.3 Further Work

The work presented in this thesis presents part of the jigsaw in bringing the Hybrid HVDC Transformer and HD-MMC to the market; however, further research is required to fill in the missing pieces. This section outlines the further work that the ORE Catapult has planned over the coming months and years to develop these concepts and attract industry support. A rough timeline for each of these projects is presented in Fig. 7.1 with the details of each project outlined in more detail below.

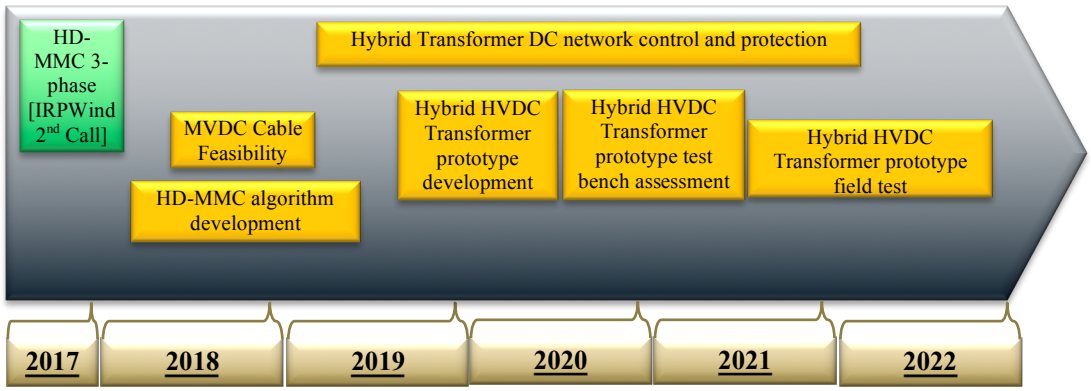


Fig. 7.1 Timeline of future works, green-funding won, yellow-funding yet to be secured

7.3.1 HD-MMC Further Work

7.3.1.1 IRPWind Second Call

The HD-MMC experiments verified the correct operation of the HD-MMC algorithm and showed it has potential benefits over using PWM with a C-MMC for applications where the number of SMs per arm is constrained. To simplify the experiment and focus the results on the performance of the HD-MMC, the high-level control functions of the MMC were omitted and only 1-phase of the converter was used. While this was effective at verifying the operation of the HD-MMC algorithm, it does not represent a realistic case.

To address this, a consortium including ORE Catapult, SINTEF, IREC and Technalia was assembled and a second experiment devised using the funding won from the second European call of the IRPWind programme. The experiment will assess the HD-MMC using the four cases listed below to demonstrate its viability for the next generation of offshore wind turbines.

1. Constant DC/AC grid conditions.
2. Dynamic response.
3. Steady state grid side converter operation.
4. Steady state generator side converter operation.

In the first case, the HD-MMC will be provided with a constant DC and stable AC grid connection. The capacitor voltage ripples, AC and arm voltages and currents as well as the power transferred will be analysed to verify the correct operation of the HD-MMC. The second case will then characterise the response of the HD-MMC to sudden disturbances to evaluate its stability. The converter will be subjected to step changes in the real and reactive power Set points as well as sudden changes in the AC grid voltage, phase and frequency as specified by the IEC 61400-21-1 standard [165] and UK grid code [166]. The response time and stability of the HD-MMC will then be analysed to assess its performance.

The third case will evaluate the HD-MMC for use as a grid-facing converter under realistic steady state conditions. Using the IEC 61400-21-1 standard in tandem with the UK Grid Code, a realistic 3-phase AC time series will be created. The grid emulator at SINTEF will then be used to generate the time series at the AC terminals of the HD-MMC. The capacitor voltages, arm currents and voltages as well as power transferred and AC terminal voltages will be monitored to verify the continued stable operation of the HD-MMC.

Finally, the HD-MMC will be subjected to the voltage and current waveforms seen by the generator side converters on offshore wind turbines. High resolution measurement equipment has been installed on the Levenmouth Demonstration Turbine (LDT) owned by ORE Catapult. These will be used to record the voltages and currents at the generator's AC terminals prior to being rectified by the converter. The results of this measurement campaign will be scaled down to create a time series file as an input to the grid emulator.

7.3.1.2 HD-MMC Algorithm Development

In Section 5.2, some limitations of the HD-MMC were revealed and in Section 5.3, two possible additions to the HD-MMC were briefly introduced. Both these options are planned to be developed and tested in the HD-MMC algorithm development project occurring in 2018. Detailed models will be built in the MATLAB/Simulink environment, after which the additions to the HD-MMC will be validated experimentally.

To date the work on the HD-MMC has focused on the HB-MMC topology as this was the original configuration introduced in 2001. In principle, the HD-MMC algorithm can be equally applied to other MMC topologies including the full bridge topology although this is yet to be

verified. The HD-MMC algorithm may even perform better here as there are additional redundant states created by the reversible SM polarity. This project will also investigate the use of the HD-MMC in different MMC configurations through simulation and experimental validation.

7.3.2 MVDC Cable Testing

This thesis focusses on the development and optimisation of the Hybrid HVDC Transformer; however, the technology to bring this to market is likely still some time off. A reasonable intermediary step would be to us the Hybrid Transformer concept in MVDC network first. Unfortunately, there is no MVDC industry yet. This could provide an important method to reduce the cost of offshore wind in the transition between HVDC and long-distance AC transmission.

One of the major obstacles to the initialisation of the MVDC market is the absence of a MVDC cable and the main reasons for cable manufactures not supplying MVDC cables is that there is currently no market for them. One way to tackle this "chicken and egg" situation is to use 33 kV or 66 kV AC cables to start the market. It has been suggested that using AC cables for DC applications can damage the insulation and significantly reduce cable life; however, the cable construction is very similar. The similarity has led National Grid to conduct a field test in North Wales where an existing AC cable connection has been upgraded to MVDC using the original AC cables. While the cable is currently operated below its rated value to mitigate potential issues, experimental studies on the effects of running DC in AC cables could allow future projects to use the full cable rating.

The ORE Catapult will address this hole through the MVDC cable testing project. By partnering with a 66 kV cable manufacturer, ORE Catapult will provide the cable testing facilities necessary to perform the necessary full scale tests to validate computer models. Additionally, the project will explore by what extent the lifetime of the AC cable will be reduced through use with DC and what can be done to mitigate this.

7.3.3 Hybrid HVDC Network Control and Protection

This project has focused primarily on the component level of the Hybrid HVDC Transformer concept. Before the concept can be used commercially, the DC network control and protection angle must also be addressed. While there are many projects looking at DC networks for

offshore wind, they are primarily concerned with connecting wind farms together. The network required for the Hybrid HVDC Transformer differs significantly from this however. In this example, the power is primarily unidirectional (from the turbines to shore). Furthermore, the power level is much lower and so different protection strategies can be considered. Lastly, there is no unifying control point offshore such as the offshore HVDC substation, the power control options considered will therefore likely differ significantly.

7.3.4 Hybrid HVDC Transformer Prototype and Testing

The next steps in the Hybrid HVDC (or MVDC) Transformer will involve prototype development. To be relevant to industry, the prototype will be developed in close collaboration with industry. The prototype will be commissioned and preliminary tests will be conducted within ORE Catapult's 15 MW powertrain test facility (Fujin) after the 17 MW eGrid system has been fully commissioned. After the successful demonstration of the Hybrid Transformer in Fujin, it will be incorporated into the 7 MW LDT facility for field testing.

Appendix A **Bibliography**

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Appendix B Current Control Derivation

This section provides a detailed derivation of the current control discussed in Section 2.1.3.2. For clarity, the derivation is covered from start to finish below although parts are already covered in Section 2.1.3.2. To derive the current control, a simplified model of the MMC must first be created. In the simplified topology, it is assumed that the arm SMs can be represented by a sinusoidal voltage sources (u_{pj} and u_{nj}) with a $1/2U_{dc}$ voltage offset (Fig. B.1). The arm resistors R_0 represent the resistive losses of the IGBTs and arm inductors L_0. The DC bus is modelled by the two DC sources (U_{dc}/2) and the

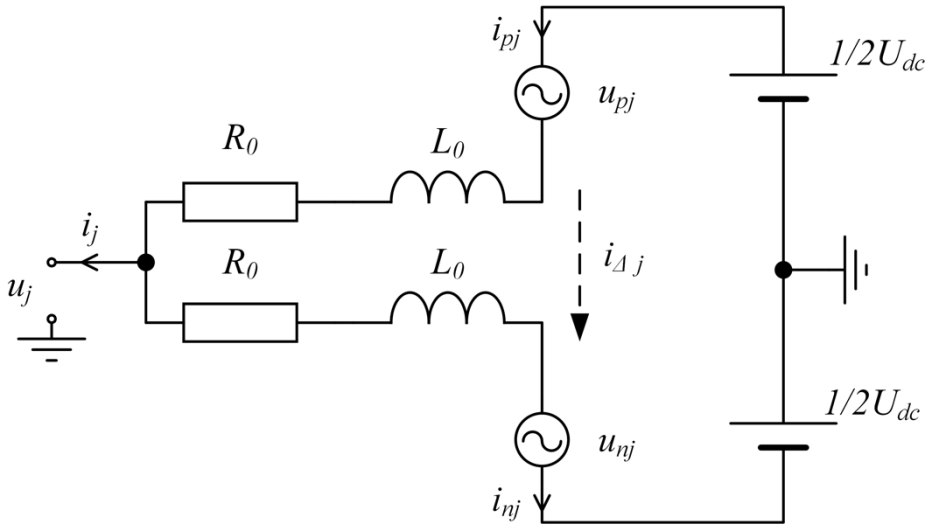

Fig. B.1 3-phase simplified MMC circuit diagram

From Fig. B.1 it is possible to derive expressions for the arm currents (i_{pj} and i_{nj}) of the j^{th} phase in terms of the AC terminal current, i_j and a difference current $i_{\Delta j}$. This difference current

is a circulating current that flows through the converter arms but does not appear on the AC or DC terminals.

$$i_{pj} = i_{\Delta j} + \frac{1}{2} i_j \tag{B.1}$$

$$i_{nj} = i_{\Delta j} - \frac{1}{2} i_j \tag{B.2}$$

Where:

$$i_{\Delta j} = \frac{i_{pj} + i_{nj}}{2} \tag{B.3}$$

The AC terminal voltage, u_j can also be derived from Fig. B.1 as follows:

$$u_j = \frac{U_{dc}}{2} - R_0 i_{pj} - L_0 \frac{di_{pj}}{dt} - u_{pj} \tag{B.4}$$

$$u_j = -\frac{U_{dc}}{2} + R_0 i_{nj} + L_0 \frac{di_{nj}}{dt} + u_{nj} \tag{B.5}$$

If equations (B.1) to (B.3) are inserted into a summation of (B.4) and (B.5) it is possible to derive an expression for the output current as follows:

$$2u_j = \frac{U_{dc}}{2} - \frac{U_{dc}}{2} + (i_{nj} - i_{pj}) + L_0 \frac{d}{dt}(i_{nj} - i_{pj}) - u_{pj} + u_{nj} \tag{B.6}$$

$$2u_j = R_0(i_{\Delta j} - \frac{1}{2} i_j - i_{\Delta j} - \frac{1}{2} i_j) + L_0 \frac{d}{dt}(i_{\Delta j} - \frac{1}{2} i_j - i_{\Delta j} - \frac{1}{2} i_j) - u_{pj} + u_{nj} \tag{B.7}$$

$$e_j - \frac{R_0}{2} i_j - \frac{L_0}{2} \frac{di_j}{dt} = u_j \tag{B.8}$$

Where:

$$e_j = \frac{u_{nj} - u_{pj}}{2} \tag{B.9}$$

Through manipulation of (B.8) it is possible to control the power flow through the converter since:

- The voltage on the AC terminal is solely dependent on the terminal current and the difference between the voltage sources u_{nj} and u_{pj}.
- The difference between the voltage sources creates an AC voltage within the converter with the arm inductance and resistance creating a specified arm impedance to drive the current.
- If it is assumed that the grid fixes the AC terminal voltage then e_j can be used to control the output current.

Therefore, the inner current of the converter can be controlled simply by controlling e_j and standard dq0 control methods used by other VSCs can be employed. Using the sine oriented Parks transform (T), (B.8) can be transformed to the dq0 frame:

$$T^{-1}\begin{bmatrix}u_d\\u_q\\u_0\end{bmatrix} = T^{-1}\begin{bmatrix}e_d\\e_q\\e_0\end{bmatrix} - \frac{R_0}{2}T^{-1}\begin{bmatrix}i_d\\i_q\\i_0\end{bmatrix} - \frac{L_0}{2}\frac{d}{dt}\left(T^{-1}\begin{bmatrix}i_d\\i_q\\i_0\end{bmatrix}\right) \tag{B.10}$$

Then applying the product rule:

$$u_{dq0} = e_{dq0} - \frac{R_0}{2}i_{dq0} - \frac{L_0}{2}\left(T\frac{d}{dt}(T^{-1})i_{dq0} + \frac{d}{dt}(i_{dq0})\right) \tag{B.11}$$

where

$$T = \sqrt{\frac{2}{3}}\begin{bmatrix}sin(\theta) & sin(\theta-120) & sin(\theta+120)\\ cos(\theta) & cos(\theta-120) & cos(\theta+120)\\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2}\end{bmatrix} \tag{B.12}$$

$$T^{-1} = \sqrt{\frac{2}{3}}\begin{bmatrix}sin(\theta) & cos(\theta) & 1/\sqrt{2}\\ sin(\theta-120) & cos(\theta-120) & 1/\sqrt{2}\\ sin(\theta+120) & cos(\theta+120) & 1/\sqrt{2}\end{bmatrix} \tag{B.13}$$

$$\frac{d}{dt}(T^{-1}) = \omega_0\sqrt{\frac{2}{3}}\begin{bmatrix}cos\,(\theta) & -sin\,(\theta) & 0\\ cos\,(\theta-120) & -sin\,(\theta-120) & 0\\ cos\,(\theta+120) & -sin\,(\theta+120) & 0\end{bmatrix} \quad (\theta = \omega_0 t) \tag{B.14}$$

It can be then shown that (B.11) can be simplified to:

$$u_d = e_d - \frac{R_0}{2}i_d + \frac{L_0}{2}i_q\omega_0 - \frac{L_0}{2}\frac{d}{dt}(i_d) \tag{B.15}$$

$$u_q = e_q - \frac{R_0}{2}i_q - \frac{L_0}{2}i_d\omega_0 - \frac{L_0}{2}\frac{d}{dt}(i_q) \tag{B.16}$$

since under balanced conditions the 0th component is eliminated and

$$T\frac{d}{dt}(T^{-1}) = \begin{bmatrix}0 & -\omega_0 & 0\\ \omega_0 & 0 & 0\\ 0 & 0 & 0\end{bmatrix} \tag{B.17}$$

After writing (B.15) and (B.16) in the frequency domain and assuming that $R_0 << L_0$ for simplicity, the plant can be shown diagrammatically according to Fig. B.2 and expressed for i_d and i_q as:

$$i_d = \frac{1}{sL_0}(e_d - u_d + \omega_0 L i_q) \tag{B.18}$$

$$i_q = \frac{1}{sL_0}\left(e_q - u_q - \omega_0 L i_d\right) \tag{B.19}$$

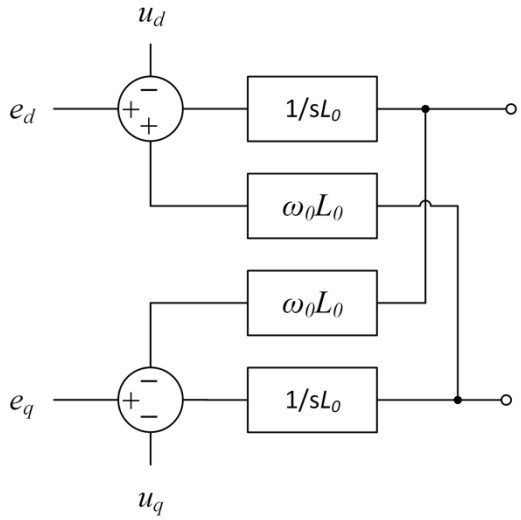

Fig. B.2 Transfer function of the plant

From (B.18) and (B.19) it is clear i_d and i_q are coupled such that controlling one will result in changes in the other. Clearly this will influence control stability and so it is advantageous to eliminate this cross coupling. The transfer function of the whole system (G_T) should therefore be derived to create a control capable of decoupling i_d from i_q.

From the diagram of the whole system, Fig. B.3, the transfer function of the plant (G_p) can be written as:

$$G_p = \frac{\vec{I}}{\overrightarrow{\Delta V}} \tag{B.20}$$

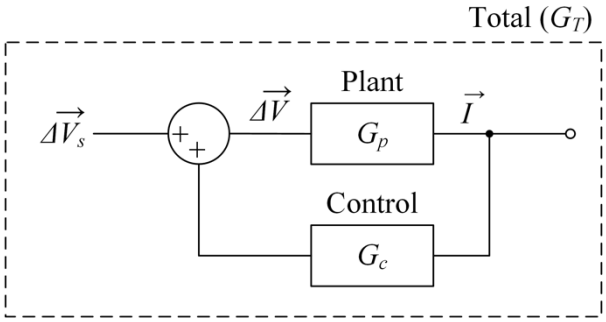

Fig. B.3 The transfer function for the whole system

It is possible to derive an expression relating $\vec{I}$ to $\overrightarrow{\Delta V}$ by summing the vectorised form of (B.18) and (B.19) and substituting $\Delta V_{dq} = e_{ed} - u_{dq}$:

$$i_d = \frac{1}{sL}\left(\Delta V_d + \omega L i_q\right) \tag{B.21}$$

$$j i_q = \frac{1}{sL}\left(j\Delta V_q - j\omega L i_d\right) \tag{B.22}$$

$$sL\left(i_d + j i_q\right) = \Delta V_d + j\Delta V_q + \omega L\left(i_q - j i_d\right) \tag{B.23}$$

$$sL\vec{I} = \overrightarrow{\Delta V} - j\omega L\vec{I} \tag{B.24}$$

where:

$$L = \frac{1}{2}L_0 \tag{B.25}$$

$$\vec{I} = i_d + j i_q \tag{B.26}$$

$$\overrightarrow{\Delta V} = \Delta V_d + j\Delta V_q \tag{B.27}$$

Therefore, inserting (B.24) into (B.20) gives G_p as:

$$G_p = \frac{\vec{I}}{\overrightarrow{\Delta V}} = \frac{1}{(SL + j\omega L)} \tag{B.28}$$

From Fig. B.3 it can be seen that G_T can be expressed as:

$$G_T = \frac{\vec{I}}{\overrightarrow{\Delta V_s}} \tag{B.29}$$

where

$$\overrightarrow{\Delta V_s} = \overrightarrow{\Delta V} - \overrightarrow{\Delta V_c} \tag{B.30}$$

and so

$$\overrightarrow{\Delta V_s} = \vec{I}\left(\frac{1}{G_p} - G_c\right) \tag{B.31}$$

$$G_T = \frac{\vec{I}}{\overrightarrow{\Delta V_s}} = \frac{G_p}{1 - G_p G_c} \tag{B.32}$$

An expression for G_c can now derived to decouple i_d and i_q by solving (B.32) by substituting (B.28) and given that $G_T = 1/sL$

$$G_c = \frac{G_T - G_p}{G_T G_p} \tag{B.33}$$

$$G_c = j\omega L \tag{B.34}$$

To decouple the converter currents G_c should cancel the cross coupling and hence have the opposite sign from the terms in (B.18) and (B.19). By combining (B.34) with (B.18) and (B.19) yields a control algorithm relating e_{dq} to the desired AC terminal current i_{dq}.

$$e_d = u_d - \frac{L}{2}\omega_0 i_q - \left[K_{p1}(i_d^* - i_d) + K_{i1}\int (i_d^* - i_d)dt\right] \tag{B.35}$$

$$e_q = u_q + \frac{L}{2}\omega_0 i_d - \left[K_{p2}(i_q^* - i_q) + K_{i2}\int (i_q^* - i_q)dt\right] \tag{B.36}$$

Appendix C Current Suppression Control Derivation

This appendix concerns the derivation of the circulating current control. For clarity, the derivation is covered from start to finish below although parts are already covered in Section 2.1.3.2. To derive the current control, a simplified model of the MMC must first be created. In the simplified topology, it is assumed that the arm SMs can be represented by a sinusoidal voltage sources (u_{pj} and u_{nj}) with a $1/2U_{dc}$ voltage offset (Fig. C.1). The arm resistors R_0 represent the resistive losses of the IGBTs and arm inductors L_0. The DC bus is modelled by the two DC sources ($U_{dc}/2$).

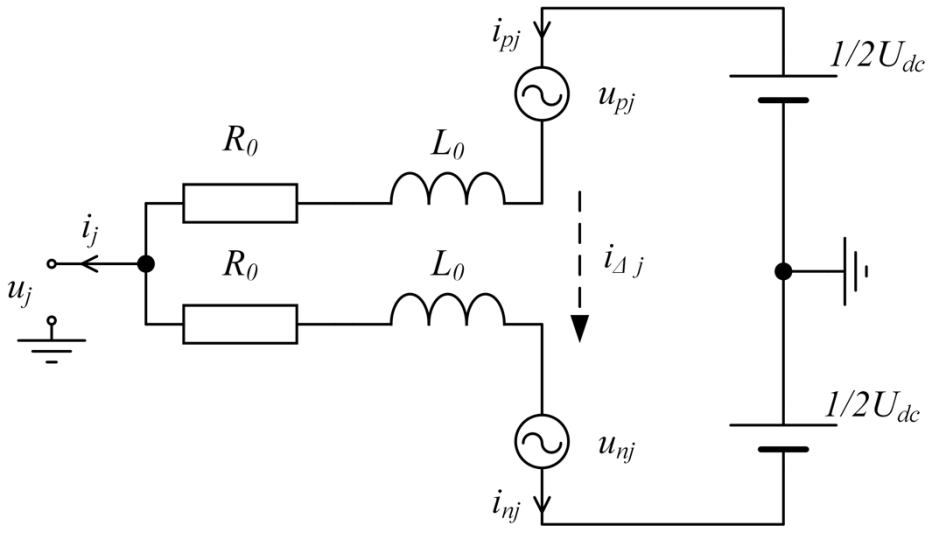

Fig. C.1 3-phase simplified MMC circuit diagram

From Fig. C.1 it is possible to derive expressions for the arm currents (i_{pj} and i_{nj}) of the j^{th} phase in terms of the AC terminal current, i_j and a difference current $i_{\Delta j}$. This difference current

is a circulating current that flows through the converter arms but does not appear on the AC or DC terminals.

$$i_{pj} = i_{\Delta j} + \frac{1}{2} i_j \tag{C.1}$$

$$i_{nj} = i_{\Delta j} - \frac{1}{2} i_j \tag{C.2}$$

Where:

$$i_{\Delta j} = \frac{i_{pj} + i_{nj}}{2} \tag{C.3}$$

The AC terminal voltage, u_j can also be derived from Fig. C.1 as follows:

$$u_j = \frac{U_{dc}}{2} - R_0 i_{pj} - L_0 \frac{di_{pj}}{dt} - u_{pj} \tag{C.4}$$

$$u_j = -\frac{U_{dc}}{2} + R_0 i_{nj} + L_0 \frac{di_{nj}}{dt} + u_{nj} \tag{C.5}$$

If (C.5) is subtracted from (C.4) and equations (C.1) to (C.3) are inserted, then it is possible to get an expression relating the difference current circulating through the arms to arm voltages.

$$\frac{U_{dc}}{2} + \frac{U_{dc}}{2} - R_0 (i_{pj} + i_{nj}) - L_0 \frac{d}{dt} (i_{pj} + i_{nj}) - u_{pj} - u_{nj} = 0 \tag{C.6}$$

$$U_{dc} - 2R_0 i_{\Delta j} - 2L_0 \frac{di_{\Delta j}}{dt} - u_{pj} - u_{nj} = 0 \tag{C.7}$$

$$\frac{U_{dc}}{2} - \frac{u_{pj} + u_{nj}}{2} = R_0 i_{\Delta j} + L_0 \frac{di_{\Delta j}}{dt} \tag{C.8}$$

From (C.8) it can be seen that the difference current does not depend on the AC terminal voltage but only the DC bus voltage and sum of the arm voltage sources. It is therefore possible to subtract a "difference voltage" from the upper and lower arms to control the difference current without affecting the AC terminal voltage. Given this, it is useful to redefine the upper arm voltage in terms of e_j and a difference voltage ($u_{\Delta j}$).

$$\frac{U_{dc}}{2} - \frac{u_{nj}}{2} - \frac{u_{pj}}{2} + u_{pj} - u_{pj} = R_0 i_{\Delta j} + L_0 \frac{di_{\Delta j}}{dt} \tag{C.9}$$

$$u_{pj} = \frac{U_{dc}}{2} - u_j - u_{\Delta j} \tag{C.10}$$

and the lower arm voltage

$$\frac{U_{dc}}{2} - \frac{u_{nj}}{2} - \frac{u_{pj}}{2} + u_{nj} - u_{nj} = R_0 i_{diffj} + L_0 \frac{di_{diffj}}{dt} \tag{C.11}$$

$$u_{nj} = \frac{U_{dc}}{2} + e_j - u_{\Delta j} \tag{C.12}$$

Where:

$$u_{\Delta j} = R_0 i_{\Delta j} + L_0 \frac{di_{\Delta j}}{dt} \tag{C.13}$$

It is known that the difference current has a DC and double line frequency component and as such can be written as:

$$i_{diffa} = \frac{I_{dc}}{3} + I_{2f} sin\,(2\omega_0 + \varphi_0) \tag{C.14}$$

$$i_{diffb} = \frac{I_{dc}}{3} + I_{2f}\, sin\left(2\omega_0 + \frac{2\pi}{3} + \varphi_0\right) \tag{C.15}$$

$$i_{diffc} = \frac{I_{dc}}{3} + I_{2f} sin\left(2\omega_0 - \frac{2\pi}{3} + \varphi_0\right) \tag{C.16}$$

From equations (C.14)-(C.16) it is clear that the difference current is also in the negative rotation. Therefore, Park's Transform should be performed on (C.13) to yield:

$$u_{\Delta dq0} = R_0 i_{\Delta dq0} - L_0 \left(T \frac{d}{dt}(T^{-1}) i_{\Delta dq0} + \frac{d}{dt}\left(i_{\Delta dq0}\right) \right) \tag{C.17}$$

Since it is in the negative sequence, double line frequency ($\theta = -2\omega_0 t$), the result is:

$$\frac{d}{dt}(T^{-1}) = -2\omega_0 \sqrt{\frac{2}{3}} \begin{bmatrix} cos\,(\theta) & -sin\,(\theta) & 0 \\ cos\,(\theta - 120) & -sin\,(\theta - 120) & 0 \\ cos\,(\theta + 120) & -sin\,(\theta + 120) & 0 \end{bmatrix} \tag{C.18}$$

simplify to become:

$$T \frac{d}{dt}(T^{-1}) = \begin{bmatrix} 0 & 2\omega_0 & 0 \\ -2\omega_0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{C.19}$$

Inserting (C.19) into (C.17) and eliminating the 0th term therefore gives:

$$u_{\Delta d} = R_0 i_{\Delta d} + 2\omega_0 L_0 i_{\Delta q} + L_0 \frac{d}{dt}(i_{\Delta d}) \tag{C.20}$$

$$u_{\Delta q} = R_0 i_{\Delta q} - 2\omega_0 L_0 i_{\Delta d} + L_0 \frac{d}{dt}\left(i_{\Delta q}\right) \tag{C.21}$$

If, as with the current control, (C.20) and (C.21) are converter to the frequency domain and it is once again assumed that $R_0 << L_0$ then:

$$u_{\Delta d} = L_0 s i_{\Delta d} + 2\omega_0 L_0 i_{\Delta q} \tag{C.22}$$

$$u_{\Delta q} = L_0 s i_{\Delta q} - 2\omega_0 L_0 i_{\Delta d} \quad \text{(C.23)}$$

Using the same method as Appendix B to calculate the whole system and plant transfer functions to then derive a control transfer function to decouple the d and q vectors in (C.22) and (C.23) a control algorithm can be created.

$$u_{\Delta d} = L_0 s i_{\Delta d} - 2\omega_0 L_0 i_{\Delta q} \quad \text{(C.24)}$$

$$u_{\Delta q} = L_0 s i_{\Delta q} + 2\omega_0 L_0 i_{\Delta d} \quad \text{(C.25)}$$

Appendix D **SM Capacitance Derivation**

This appendix concerns the derivation of the SM capacitor size. For clarity, the derivation is covered from start to finish below although parts are already covered in Section 2.1.3.4. An expression relating the arm energy (E_{arm}) to the SM capacitance is shown in (D.1).

$$E_{arm} = \frac{1}{2} m C_{mod} u_c^2(t) \tag{D.1}$$

Inserting terms for the percentage voltage deviation Δu from a nominal value (U_c) and the maximum and minimum energy deviation ($\Delta\hat{E}_{arm}$ and $\Delta\check{E}_{arm}$ from the initial value (E_{arm_0}) provides expressions for maximum and minimum stored energy in the arm.

$$E_{arm_0} + \Delta\hat{E}_{arm} = \frac{1}{2} m C_{mod} (U_c(1 + \Delta u_c)^2) \tag{D.2}$$

$$E_{arm_0} + \Delta\check{E}_{arm} = \frac{1}{2} m C_{mod} (U_c(1 - \Delta u_c)^2) \tag{D.3}$$

The difference between the maximum and minimum stored energy in the arm (ΔE_{arm}) can then be described as:

$$\Delta E_{arm} = \Delta\hat{E}_{arm} - \Delta\check{E}_{arm} \tag{D.4}$$

If (D.2) and (D.3) are then inserted into (D.4) it yields:

$$\Delta E_{arm} = \left[\frac{1}{2} m C_{mod} \left(U_c(1 + \Delta u_c)\right)^2 - E_{a_0}\right] - \left[\frac{1}{2} m C_{mod} \left(U_c(1 - \Delta u_c)\right)^2 - E_{arm_0}\right] \tag{D.5}$$

$$\Delta E_{arm} = \frac{1}{2} m C_{mod} U_c^2 [(1 + \Delta u_c)^2 - (1 - \Delta u_c)^2] \tag{D.6}$$

$$\Delta E_{arm} = \frac{1}{2} m C_{mod} U_c^2 4 \Delta u_c \tag{D.7}$$

$$C_{mod} = \frac{\Delta E_{arm}}{2 m U_c^2 \Delta u_c} \tag{D.8}$$

So now the SM capacitance is given in terms of the energy deviation for the arm but what is wanted is an expression relating the capacitance to the voltage deviation. Therefore, an expression relating the stored energy fluctuations to the voltage ripple is required.

From Fig. 2.7 the power exchange for the upper arm can be written as:

$$P_{arm} = u_{jp} i_{jp} \tag{D.9}$$

If the AC terminal voltage u_j, current i_j, and apparent power are expressed as:

$$u_j = \Delta u_j \widehat{U}_j sin\,(\omega_0 t) \tag{D.10}$$

$$i_j = \frac{\hat{I}_j}{\Delta u_j} sin\,(\omega_0 t + \vartheta\,) \tag{D.11}$$

$$S = \frac{3}{2}\,\widehat{U}_j \hat{I}_j \tag{D.12}$$

where Δu_j represents the allowable AC voltage fluctuations, under grid code this should not exceed ±10% of the peak nominal voltage ($\widehat{U}_j$). Similarly, the nominal peak grid current is $\hat{I}_j$ and leads the grid voltage by ϑ. The AC terminal voltage can then be related to the DC bus voltage using the peak allowable AC voltage fluctuation ($\Delta\widehat{U}_j$) typically 1.1.

$$\widehat{U}_j = \frac{U_{dc}}{2\Delta\widehat{U}_j} \tag{D.13}$$

If it is assumed that the there is no circulating current and the converter has 3-phases, then the arm current and voltages are:

$$i_j = \frac{1}{2} i_{pj} + \frac{1}{3} i_{dc} \tag{D.14}$$

$$u_{pj} = u_j + \frac{1}{2} u_{dc} \tag{D.15}$$

Inserting (D.14) and (D.15) into (D.9) yields:

$$P_{arm} = \left(\frac{1}{2} U_{dc} - u_j\right)\left(\frac{1}{2} i_j + \frac{1}{3} i_{dc}\right) \tag{D.16}$$

Using (D.10) and (D.11) the DC current is:

$$i_{dc} = \frac{3}{2}\frac{\widehat{U}_j \hat{I}_j}{U_{dc}} cos\,(\vartheta) \tag{D.17}$$

and after combining with (D.13) the DC current is given by

$$i_{dc} = \frac{3}{4}\frac{\hat{I}_j}{\Delta\widehat{U}_j} cos\,(\vartheta) \tag{D.18}$$

Inserting (D.10), (D.11), (D.13) and (D.18) into (D.16) yields:

$$p_{arm} = \left(2\frac{\Delta\widehat{U}_j \widehat{U}_j}{2} - \Delta u_j \widehat{U}_j\, sin(\omega_0 t)\right)\left(\frac{\hat{I}_j}{2\Delta u_j} sin(\omega_0 t + \theta) + \frac{1}{3}\frac{3\hat{I}_j}{4\Delta\widehat{U}_j} cos(\vartheta)\right) \tag{D.19}$$

$$p_{arm} = U_{j_{nom}} K_j \left(1 - \frac{\Delta u_j}{\Delta \widehat{U}_j} sin(\omega_0 t)\right) \frac{\hat{I}_j}{4 \Delta U_j} \left(2\, sin(\omega_0 t + \theta) + \frac{\Delta u_j}{\Delta \widehat{U}_j} cos(\vartheta)\right) \tag{D.20}$$

$$p_{arm} = \frac{S}{3} \frac{\Delta \widehat{U}_j}{2 \Delta u_j} \left(1 - \frac{\Delta u_j}{\Delta \widehat{U}_j} sin(\omega_0 t)\right) \left(2\, sin(\omega_0 t + \theta) + \frac{\Delta u_j}{\Delta \widehat{U}_j} cos(\vartheta)\right) \tag{D.21}$$

The variation of arm energy over time is therefore the integral of (D.21) over time

$$\Delta e_{arm} = \int_0^t P_{arm}(x) dx \tag{D.22}$$

$$\Delta e_{arm} = \frac{S}{3} \frac{\Delta \widehat{U}_j}{2 \Delta u_j} \int_0^t \left(1 - \frac{\Delta u_j}{\Delta \widehat{U}_j} sin(\omega_0 x)\right) \left(2\, sin(\omega_0 x + \theta) + \frac{\Delta u_j}{\Delta \widehat{U}_j} cos(\vartheta)\right) dx \tag{D.23}$$

$$\begin{aligned} \Delta e_{arm} = \frac{S}{3} \frac{\Delta \widehat{U}_j}{2 \Delta u_j} \Bigg[& \int_0^t 2\, sin(\omega_0 x + \vartheta)\, dx + \int_0^t \frac{\Delta u_j}{\Delta \widehat{U}_j} cos(\vartheta)\, dx \\ & + \int_0^t 2 \frac{\Delta u_j}{\Delta \widehat{U}_j} sin\,(\omega_0 x)\, sin(\omega_0 x + \vartheta) dx - \int_0^t \frac{\Delta u_j^2}{\Delta \widehat{U}_j^2} sin(\omega_0 x)\, cos(\vartheta)\, dx \Bigg] \end{aligned} \tag{D.24}$$

$$\begin{aligned} \Delta e_{arm} = \frac{S \Delta \widehat{U}_j}{6 \Delta u_j} \Bigg[& \int_0^t 2\, sin(\omega_0 x + \backslash vartheta\,)\, dx + \int_0^t \frac{\Delta u_j}{\Delta \widehat{U}_j} cos(\vartheta)\, dx + \frac{2}{2} \frac{\Delta u_j}{\Delta \widehat{U}_j} \int_0^t cos\,(\omega_0 x \\ & - \omega_0 x - \vartheta) - cos(\omega_0 x + \omega_0 x + \vartheta) dx - \int_0^t \frac{\Delta u_j^2}{\Delta \widehat{U}_j^2} sin(\omega_0 x)\, cos(\vartheta)\, dx \Bigg] \end{aligned} \tag{D.25}$$

$$\begin{aligned} \Delta e_{arm} = \frac{S \Delta \widehat{U}_j}{6 \Delta u_j} \Bigg[& -\frac{2}{\omega} cos(\omega_0 x + \vartheta) + x \frac{\Delta u_j}{\Delta \widehat{U}_j} cos(\vartheta) - x \frac{\Delta u_j}{\Delta \widehat{U}_j} cos(\vartheta) \\ & + \frac{\Delta u_j}{\Delta \widehat{U}_j} \frac{1}{2\omega_0}\, sin(2\omega_0 x + \vartheta) + \frac{\Delta u_j^2}{\omega_0 \Delta \widehat{U}_j^2} cos(\omega_0 x)\, cos(\vartheta) \Bigg]_0^t \end{aligned} \tag{D.26}$$

$$\begin{aligned} \Delta e_{arm} = \frac{S \Delta \widehat{U}_j}{12 \omega_0 u_j} \Bigg[& -4\, cos(\omega_0 x + \vartheta) + \frac{\Delta u_j}{\Delta \widehat{U}_j}\, sin(2\omega_0 x + \vartheta) \\ & + \frac{\Delta u_j^2}{\Delta \widehat{U}_j^2} (cos(\omega_0 x - \vartheta) + cos(\omega_0 x + \vartheta)) \Bigg]_0^t \end{aligned} \tag{D.27}$$

$$\begin{aligned} \Delta e_{arm} = & \frac{S \Delta \widehat{U}_j}{12 \omega_0 u_j} \Bigg[-4\, cos(\omega_0 t + \vartheta) + \frac{\Delta u_j}{\Delta \widehat{U}_j}\, sin(2\omega_0 t + \vartheta) \\ & + \frac{\Delta u_j^2}{\Delta \widehat{U}_j^2} (cos(\omega_0 t - \vartheta) + cos(\omega_0 t + \vartheta)) \Bigg] \\ & - \frac{S \Delta \widehat{U}_j}{12 \omega_0 u_j} \left[-4\, cos(\vartheta) + \frac{\Delta u_j}{\Delta \widehat{U}_j}\, sin(\vartheta) + 2 \frac{\Delta u_j^2}{\Delta \widehat{U}_j^2} cos(\vartheta) \right] \end{aligned} \tag{D.28}$$

$$\begin{aligned} \Delta e_{arm} = \frac{S \Delta \widehat{U}_j}{12 \omega_0 u_j} \Bigg[& \frac{\Delta u_j^2}{\Delta \widehat{U}_j^2} cos(\omega_0 t - \vartheta) + \frac{\Delta u_j^2}{\Delta \widehat{U}_j^2} cos(\omega_0 t + \vartheta) - 4\, cos(\omega_0 t + \vartheta) \\ & + \frac{\Delta u_j}{\Delta \widehat{U}_j}\, sin(2\omega_0 t + \vartheta) - \frac{\Delta u_j}{\Delta \widehat{U}_j}\, sin(\vartheta) - 2 \frac{\Delta u_j^2}{\Delta \widehat{U}_j^2} cos(\vartheta) + 4\, cos(\vartheta) \Bigg] \end{aligned} \tag{D.29}$$

$$\Delta e_{arm} = \frac{S\Delta\widehat{U}_j}{12\omega_0 u_j}\left[\frac{\Delta u_j^2}{\Delta\widehat{U}_j^2}cos(\omega_0 t-\vartheta)+cos(\omega_0 t+\vartheta)\left(\frac{\Delta u_j^2}{\Delta\widehat{U}_j^2}-4+2\frac{\Delta u_j}{\Delta\widehat{U}_j}\,sin(\omega_0 t)\right)\right.$$
$$\left.-2\,cos(\vartheta)\left(\frac{\Delta u}{\Delta\widehat{U}_j^2}+2\right)\right] \tag{D.30}$$

$$\Delta e_{arm} = \frac{S}{3\omega_0}k_c \tag{D.31}$$

where

$$k_c = \frac{\Delta\widehat{U}_j}{4\Delta u_j}\left[\frac{\Delta u_j^2}{\Delta\widehat{U}_j^2}cos(\omega_0 t-\vartheta)+cos(\omega_0 t+\vartheta)\left(\frac{\Delta u}{\Delta\widehat{U}_j^2}-4+2\frac{\Delta u_j}{\Delta\widehat{U}_j}\,sin(\omega_0 t)\right)\right.$$
$$\left.-2\,cos(\vartheta)\left(\frac{\Delta u_j^2}{\Delta\widehat{U}_j^2}+2\right)\right] \tag{D.32}$$

Clearly k_c is highly non-sinusoidal and so determining a general solution for the maximum value of (D.30) is complex. However, a numerical solution for k_c has been shown in [32] to be accurate. Also since k_c contains no power or frequency terms, the generality of the solution is largely unaffected.

The maximum energy deviation was found in [32] to be at reactive only loads (ϑ = 90°) at a power factor (pf = 0.9) and reduce at higher power factors; however, the MMC limits the max power factor to 1. Under these conditions k was found to be 2.44 and hence (D.8) can be rewritten as:

$$C_{mod} = \frac{2.44\,S}{6mU_c^2\Delta u_c} \tag{D.33}$$

Appendix E Generalisation of Dowell's Equation

Dowell's Expression is defined as:

$$R_{ac} = \frac{\rho_w l_w}{A_w} N \frac{t_w}{\delta}\left[\left(\frac{\sinh\left(2\frac{t_w}{\delta}\right)+\sin\left(2\frac{t_w}{\delta}\right)}{\cosh\left(2\frac{t_w}{\delta}\right)-\cos\left(2\frac{t_w}{\delta}\right)}\right)+\frac{2(N^2-1)}{3}\left(\frac{\sinh\left(2\frac{t_w}{\delta}\right)-\sin\left(2\frac{t_w}{\delta}\right)}{\cosh\left(2\frac{t_w}{\delta}\right)+\cos\left(2\frac{t_w}{\delta}\right)}\right)\right] \quad \text{(E.1)}$$

Dowell also proposed correction factors to generalise (E.1) such that it can be applied to windings that do not utilise the entire height of the core window, square windings and round windings. An example of how to apply the correction factor is provided here with the aid of Fig. E.1 for circular windings, as this requires the largest correction. However, equations (E.2) – (E.7) and (E.4) – (E.7) are applicable for conversion from square or short foil windings to full foil windings respectively.

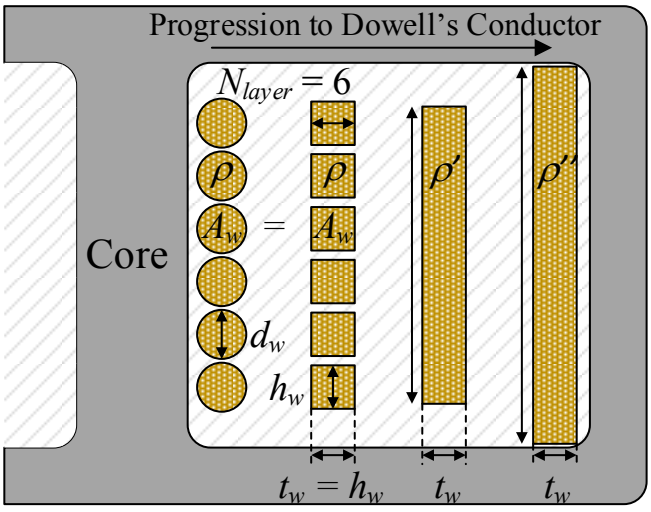

Fig. E.1 Progression of from a circular winding to full window foil for use with Dowell's Expression

Dowell's conversion method first replaces round conductors with square conductors with the same cross-sectional area i.e.

$$h_w = \sqrt{\frac{\pi}{4}} d_w \tag{E.2}$$

where h_w is the height of the equivalent square conductor. The square or rectangular windings are then replaced by an equivalent foil winding which is designed to have the same height as the original windings. Since there was insulating material between the original windings in each layer however, a new resistivity is defined for the equivalent foil such that the magnetic field along the winding path is equal.

$$\rho' = \frac{1}{\eta_w} \rho \tag{E.3}$$

Where the porosity factor η_w is calculated from the ratio of the conductor heights to the equivalent conductor height (h'_w):

$$\eta_w = \frac{N_{layer} h_w}{h'_w} \tag{E.4}$$

Finally, a second porosity factor (η'_w) is defined to create an equivalent foil conductor that utilises the entire height of the transformer core window height (h''_w) such that:

$$\eta'_w = \frac{h'_w}{h''_w} \tag{E.5}$$

And hence (E.1) can be rewritten as:

$$R_{ac} = R_{dc} \Delta \left[\left(\frac{sinh(2\Delta) + sin(2\Delta)}{cosh(2\Delta) - cos(2\Delta)} \right) + \frac{2(N^2 - 1)}{3} \left(\frac{sinh(2\Delta) - sin(2\Delta)}{cosh(2\Delta) + cos(2\Delta)} \right) \right] \tag{E.6}$$

Where Δ is given by:

$$\Delta = \eta''_w \frac{t_w}{\delta}, \qquad \eta''_w = \eta'_w \eta_w \tag{E.7}$$

Since it was proposed, the validity of using the porosity as a correction factor has been doubted but it has been found to be accurate compared to other methods for both round and square conductors [118], [119] as shown by analysis in [120], [121]. It can be seen though that as the porosity factor increases (such as in litz wires) the accuracy of Dowell's equation reduces, [120].

Appendix F AC Resistance of Litz Wire

Mathematical expressions to more accurately describe the AC resistance of litz wires are developed in [167], [168]. These expressions assume that the magnetic field strength due to the proximity effect increases linearly through the conductors of the primary windings, decreases linearly through the conductors of the secondary windings and is constant through the insulation between each winding (Fig. F.1).

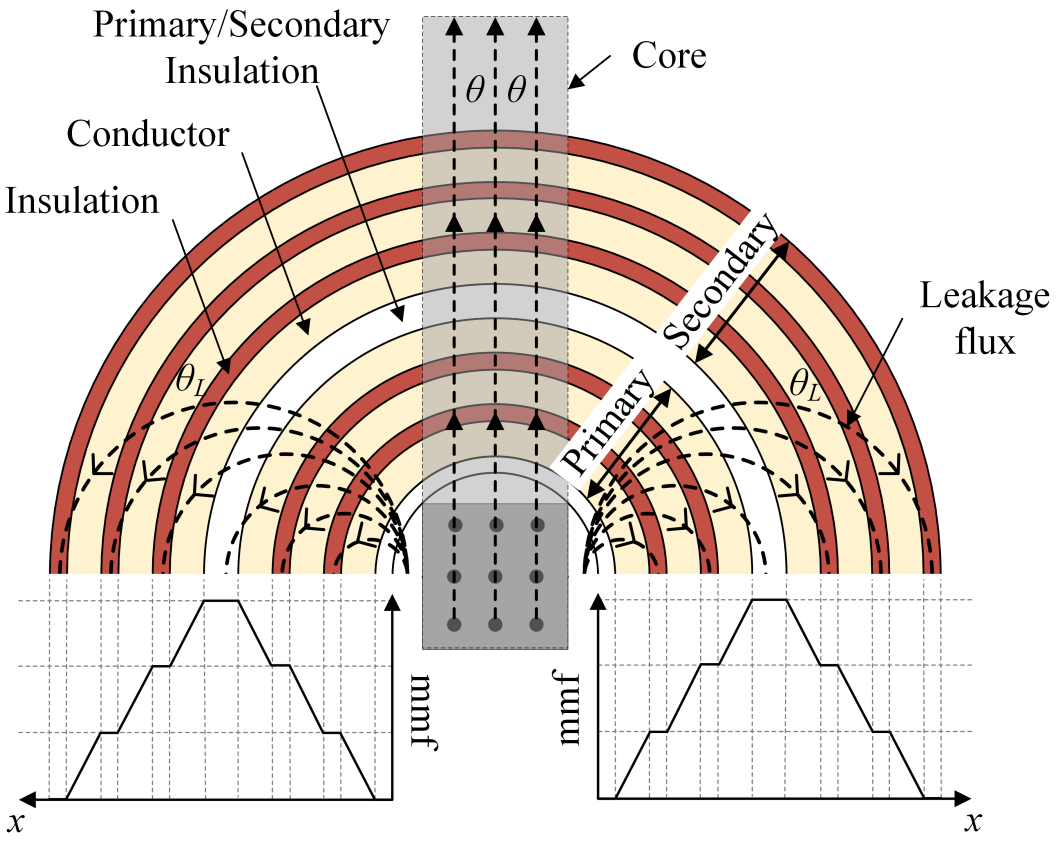

Fig. F.1 The leakage flux and resulting mmf distribution through the transformer windings

This can be derived from Ampere's Law (2.57) if it is assumed that there is an equal distribution of current density in each winding i.e. (2.72) is true. If, however, (2.72) is not true, the magnetic field strength no longer follows a trapezoidal form through the windings, as shown in Fig. F.2 from [117] and [167], [168] are no longer accurate [169].

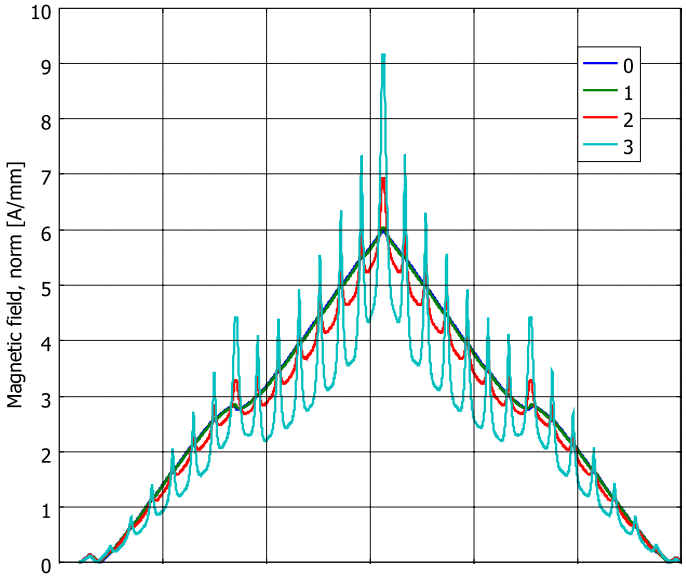

Fig. F.2 Magnetic field strength through the primary and secondary windings [117]

Since high penetration factors result in low accuracies for all methods, it is proposed in [117] that a simpler method [170] is used to calculate AC winding resistance with similar results.

$$R_{ac} = \frac{R_{dc}}{2}\left(1 + \frac{\gamma^4}{192}\left(\frac{1}{6} + \frac{\pi^2 n_s p_f}{4}\left(16m^2 - 1 + \frac{24}{\pi^2}\right)\right)\right) \tag{7.1}$$

Where n_s is the number of strands in the Litz bundle (Fig. F.3) and the packing factor (p_f) is the ratio of copper to bundle area, and can be simplified to:

$$p_f = n_s\left(\frac{r_s}{r_b}\right)^2 \tag{7.2}$$

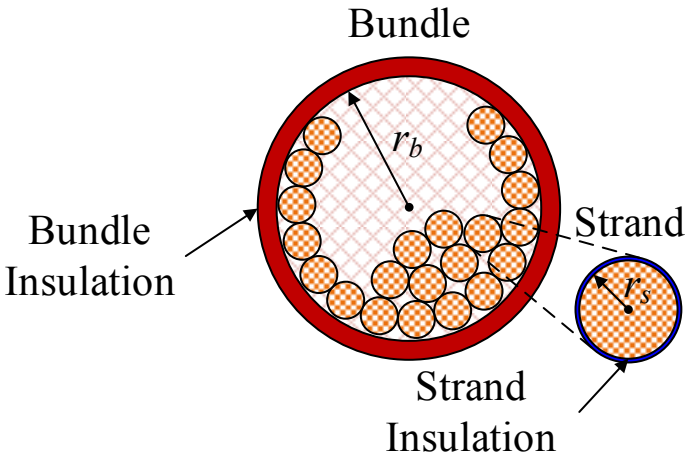

Fig. F.3 Cross Section of a litz wire with individual strands shown